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(54) Title: A HIGH-DATA-RATE WIRELESS LOCAL-AREA NETWORK

(57) Abstract

An apparatus and method for communicating data between at least two data devices, suitable for use as a wireless local-area network, that provides robust data communication via a radio communication channel corrupted by multipath interference, particularly at high data rates. A preferred embodiment of the invention represents data as a sequence of Walsh-function waveforms (66) encoded by pseudo-noise direct-sequence spread-spectrum modulation (70). Walsh function encoding of the data provides a long symbol duration, thereby allowing the spread spectrum modulation to provide processing gain sufficient to substantially overcome multipath interference, while providing a high data rate.

A HIGH-DATA-RATE WIRELESS LOCAL-AREA NETWORK

1   **Field of the Invention**

2   This invention relates generally to wireless local-area networks, and more

3   particularly to wireless local-area networks for use in high-data-rate applications

4   subject to multipath interference.

5

6   **Background of the Invention**

7   Computer communications networks for allowing computers to communicate

8   data to and from other computers have become common. For example, a user of a

9   first computer can send and receive files and real-time data to and from a second

10 computer. A local-area network (LAN) is a computer communications network

11 which provides computer communications among a plurality of computers situated

12 within a common locale. For example, a LAN is typically used to interconnect

13 personal computers or workstations within an office or school building, or to

14 interconnect computers situated in several buildings of a campus or office park. The

15 computers connected to the LAN typically communicate among one another, and

16 usually also communicate with one or more centralized or specialized computers,

17 such as a host computer, with an output device, such as a printer, and with a mass

18 data storage device, such as a file server.

19   A computer communications network, such as a LAN, employs a

20 transmission medium to communicate data signals among the plurality of data

21 devices in the network. Usually, the transmission medium is a network of wires.

22 Wires can be cumbersome in that they can present routing problems, occupy space,

23 require installation time, and inhibit the mobility of the computers connected to the

24 network.

25   To overcome the problems associated with using a system of wires as the

26 transmission medium, a plurality of radio transceivers can be used to communicate

27 radio signals for carrying data messages among the computers in the computer

28 communications network. Use of radio transceivers has gained little acceptance so

29 far due to low data transmission rates and/or unreliability. Typically, if the data

1   transmission rate is lowered, the reliability can be improved. Alternatively, high data

2   transmission rates can be achieved, albeit with reduced reliability.

3   The principle barrier to high data rate communications between computers in

4   a wireless local-area network is an interference phenomenon called "multipath". A

5   radio signal commonly traverses many paths as it travels towards a receiver.

6   Multiple propagation paths can be caused by reflections from surfaces in the

7   environment, for example. Some of these paths are longer than others. Therefore,

8   since each version of the signal travels at the same speed, some versions of the

9   signal will arrive after other versions of the signal. Sometimes the delayed signals

10   will interfere with more prompt signals as the delayed signals arrive at the receiver,

11   causing signal degradation.

12   Multipath time-delay spread is the time that elapses between the moment that

13   the earliest version of a transmitted signal arrives at a receiver, and the moment that

14   the latest version of the signal arrives at the receiver.

15   To understand multipath effects and the instant invention, it is helpful to

16   discuss the term "symbol". One or more symbols can be combined to form a

17   message that conveys meaning. Each symbol must be uniquely recognizable, and is

18   selected from a set of possible symbols, referred to as a symbol alphabet. The

19   number of symbols in the symbol alphabet is referred to as the "order" of the symbol

20   alphabet. For example, the letters "a", "b", and "c" are symbols from the English

21   alphabet, where the order of the English alphabet is 26. The numbers "0" and "1"

22   are symbols of the binary number system, which is of order 2.

23   It is possible to represent a sequence of symbols from a first alphabet with

24   a symbol from a second alphabet, such as representing the binary symbol sequence

25   "101" by the symbol "a". This binary symbol sequence consists of three binary

26   symbols. Since each binary symbol can be either one of two possible symbols, in a

27   sequence of three binary symbols, there are eight possible unique binary symbol

28   sequences. Thus, an alphabet of order eight is required to represent the eight

29   possible unique binary symbol sequences of three symbols each. In general, an

30   alphabet of order $M = 2^N$ is required to represent the $M = 2^N$ possible unique

31   binary symbol sequences of N symbols each.

1   Just as binary signalling can be referred to as 2-ary signalling, a signalling

2   system that represents three-element binary symbol sequences using a symbol

3   alphabet of order eight is referred to as 8-ary signalling. In the terminology of

4   communications system design, an 8-ary symbolic representation is said to represent

5   each symbol using "3 bits per symbol".

6   In general, a signaling system that represents an N-element binary symbol

7   sequence using a symbol alphabet of order $M = 2^N$ is referred to as M-ary

8   signalling. In M-ary signalling, the equivalent binary data rate R is the symbol rate

9   S multiplied by the number of bits per symbol N, i.e., $R = S * N$. The number of

10   bits per symbol N is $\log_2 M$. Thus, for 8-ary signalling, $N = 3$, and therefore the

11   equivalent binary data rate is three times the symbol rate (assuming no error

12   correction coding and no overhead bits).

13   In binary signalling, the equivalent binary data rate is equal to the symbol

14   rate, i.e, $R = S$, because when $M = 2$, the number of bits per symbol N is one.

15   Consequently, "bit" and "symbol" are often used interchangeably in discussions of

16   binary signalling.

17   In radio communications, a transmitter includes a modulator that provides a

18   transmitted signal representative of information presented to the modulator.

19   Conversely, a receiver includes a demodulator that receives the transmitted signal

20   and ideally provides the original information represented by the transmitted signal.

21   Commonly, the information presented to the modulator includes a plurality of

22   symbols, where each symbol is selected from a finite set of symbols. For each

23   symbol presented to the modulator, the modulator generates a corresponding symbol

24   waveform selected from a set of discrete symbol waveforms, the symbol waveform

25   then being transmitted over a communications channel to be received by at least one

26   receiver.

27   Each symbol waveform that is transmitted is subject to distortion and noise,

28   thereby making each received symbol waveform differ from the corresponding

29   original transmitted symbol waveform, and become more similar to other symbol

30   waveforms that were not actually transmitted. Consequently, it is necessary to decide

31   which symbol of the discrete set of known symbols was most likely transmitted. This

32   decision is performed in the demodulator of the receiver, the output of the

1   demodulator being a sequence of symbols, selected from the known set of symbols,

2   that represents the best estimation of the transmitted symbol sequence.

3   To decide which symbol sequence has been transmitted, for each transmitted

4   symbol, the demodulator processes the corresponding received symbol waveform for

5   a period of time called a coherent integration interval. It is essential that each

6   coherent integration interval be coincident with each received symbol waveform,

7   thereby providing correct synchronization. In the absence of correct synchronization,

8   the symbol content of the received waveform will be misinterpreted.

9   To further clarify the concept of multipath interference, consider the case of

10   a message transmitted as a binary data modulation waveform, wherein each message

11   symbol consists of a single bit. When the multipath time-delay spread is longer than

12   the duration of a symbol waveform, symbol waveforms of the first version of the

13   received signal overlap non-corresponding symbol waveforms of the excessively

14   delayed versions of the received signal. This phenomena is called intersymbol

15   interference (ISI).

16   For example, in a typical indoor or campus radio network environment, the

17   time-delay spread can be greater than 500 nanoseconds (ns). Since in binary data

18   modulation, data rate is the multiplicative inverse (reciprocal) of symbol duration,

19   a time delay spread of 500 ns implies that data rates even much less than two million

20   bits per second (Mbps) will result in significant data errors due to intersymbol

21   interference.

22   In addition to intersymbol interference, some multipath reflections may

23   exhibit time-delay spreads that are less than the duration of a symbol waveform. This

24   form of multipath interference is referred to as intrasymbol interference, and such

25   interference can cause a significant degradation in the amplitude of the total received

26   signal.

27   In intrasymbol interference, the multipath time-delay spread is shorter than

28   the duration of a symbol waveform. Thus, symbol waveforms of the first received

29   signal version overlap non-corresponding portions of corresponding symbol

30   waveforms of the delayed versions of the received signal. Consequently, reflected

31   signals of significant amplitude will cause periodic amplitude nulls in the frequency

32   spectrum of the total received signal due to coherent cancellation at particular

1   frequencies. The bandwidth of the amplitude nulls is inversely proportional to the

2   delay of the corresponding signal that is causing the interference. This phenomenon

3   is known as "frequency selective fading", and it substantially impairs the reliability

4   of communication between a transmitter and a receiver.

5   Overcoming frequency selective fading is commonly accomplished using

6   diversity methods. These methods include spatial diversity, polarization diversity,

7   and frequency diversity. Spatial and polarization diversity require at least two

8   receivers, each having a separate receive antenna, such that the frequency selectivity

9   pattern is different for each antenna.

10   Frequency diversity receivers can share a single broadband receive antenna,

11   but the transmitted signal is duplicated and is transmitted on at least two carrier

12   signals that are separated by a frequency bandwidth that is larger than the width of

13   a frequency null. A frequency diversity receiver unit consists of multiple receivers,

14   each tuned to a different carrier frequency. The receiver outputs of either method

15   fade independently, and are combined in one of several known ways to take

16   advantage of this. Since this method employs an independent receiver for each

17   diversity channel used, it can be quite costly to implement.

18   There are known methods for reducing intersymbol interference due to

19   multipath effects while preserving high data rates. A first method employs highly

20   directional line-of-sight microwave links with high antenna gain, since signals having

21   the longest delays often arrive at angles far from the central axis of the microwave

22   antenna. One problem with this method is that to obtain high antenna gain, the

23   antennas must be large, mounted on fixed platforms, and must be carefully pointed.

24   Such antennas are therefore complicated and expensive to install and move. Large

25   antennas are particularly unsuitable for short range indoor or campus environments.

26   A second method for reducing intersymbol interference due to multipath

27   effects while preserving high data rates is to use echo canceling techniques

28   implemented using adaptive filters. However, the expense and computational

29   requirements of adaptive filters is prohibitive at the high data rates required in the

30   highly dynamic environment of radio communications.

31   A third method is to channelize the transmitted waveform into multiple

32   channels, each channel being of different carrier frequency and of lower bandwidth

1   (therefore using longer symbol durations) than the single-channel transmitted

2   waveform. Each channel is then received independently. This approach is excessively

3   costly because one independent receiver per channel is required.

4   A fourth and less conventional approach is to use M-ary orthogonal

5   signalling, with symbols that are $\log_2 M$ times as long as the binary symbols would

6   be. According to the property of orthogonality, the waveform that represents each

7   symbol has no projection on the respective waveform of any other symbol of the

8   symbol alphabet from which the symbols of the message are selected. Consequently,

9   each symbol in the alphabet is more easily distinguished from other symbols in the

10   alphabet than without the orthogonality property.

11   If the temporal symbol duration of the orthogonal signal is made much longer

12   than the multipath time delay spread, the effect of the multipath can be reduced. For

13   example, one of many approaches includes the use of M-ary frequency shift keying

14   (MFSK) modulation to encode the high-order symbol alphabet into one of M

15   frequencies. Orthogonal signaling would still require a diversity receiver to overcome

16   intrasymbol interference. Furthermore, orthogonal signalling requires excessive

17   bandwidth to implement as compared with a conventional communications channel,

18   and is therefore typically prohibited by government regulation.

19   All of these approaches for reducing intersymbol interference due to multipath

20   effects while preserving high data rates must, in general, also include means for

21   diversity reception to reduce the <u>intra</u>symbol interference, and consequently must

22   employ duplicate receivers.

23   Direct-sequence spread spectrum (DSSS) modulation is a multiplicative

24   modulation technique that can be used for resolving and discriminating against

25   multipath interference. A common but unsatisfactory approach to mitigating

26   multipath effects is to employ direct-sequence spread spectrum modulation in

27   conjunction with binary data modulation, where the direct-sequence spreading

28   function of the DSSS modulation is a pseudonoise (PN) waveform. This approach

29   is unsatisfactory because it cannot provide sufficiently high data rates to support

30   LAN throughput requirements when sufficient processing gain is used for

31   overcoming multipath effects.

1   The processing gain of a binary-data-modulated spread spectrum waveform

2   is the ratio of the spreading bandwidth of the DSSS modulation to the data

3   bandwidth. The spreading bandwidth is often limited due to constraints imposed by

4   government regulation or by shortcomings of signal processing technology. Lowering

5   the binary data rate increases processing gain and consequently robustness. but

6   sacrifices rate of data throughput.

7   The ability to reduce both intersymbol and intrasymbol interference due to

8   multipath effects depends on the processing gain of the spread spectrum waveform

9   and receiver, whereas the ability to resolve adjacent paths is a function only of the

10   spreading bandwidth, not of the symbol rate.

11   It is known to use Walsh-function waveforms to implement code division

12   multiple access (CDMA). CDMA is used to improve the channel capacity of a

13   spread spectrum system where multiple transmitters share the same frequency

14   spectrum. Walsh-function modulation is used to provide separable signals. It is

15   difficult to ensure this separability because of limited processing gain, and hence

16   precise transmitter power regulation is usually required. Further improvements in

17   gain would be desirable.

18   Gilhousen, US Patent 5,103,459, specifically teaches a cellular telephone

19   system that employs spread spectrum encoding to discriminate among the signals of

20   multiple users. This capability illustrates a well-known CDMA application of spread

21   spectrum signalling. Reduction of multipath interference is not addressed. In the

22   forward channel, Walsh-function signalling is used for improved CDMA

23   performance, not for data modulation. Furthermore, Walsh-function signalling is not

24   used to increase the CDMA processing gain by extending the symbol duration. but

25   only to provide a better CDMA waveform than pseudo-noise DSSS would alone

26   provide, because the treatment is such that the orthogonality property occurs between

27   multiple users sharing the same frequency band, and not between data symbols.

28   Although Gilhousen '459 discusses the use of Walsh-function data modulation in the

29   reverse channel, Gilhousen '459 clearly states that the purpose of the Walsh-function

30   signalling is to obtain good Gaussian noise performance in a Rayleigh fading

31   multipath channel. Consequently, use of a modulation, such as binary phase shift

32   keying, that requires a coherent phase reference signal for demodulation is

1   precluded. Gilhousen '459 states that differential phase shift keying will not operate
2   well in a Rayleigh fading multipath environment, and some means of orthogonal
3   signalling is required to overcome the lack of a phase reference. Moreover, since
4   the multipath channel discussed in Gilhousen '459 is Rayleigh fading, Gilhousen '459
5   does not resolve and discriminate against multipath interference. Further, the use
6   in Gilhousen '459 of Walsh-function signalling for data modulation is independent
7   of the use therein of spread spectrum encoding. Gilhousen '459 explicitly states that
8   binary orthogonal signalling also works, since a coherent phase reference would not
9   be required. The receiver described in Gilhousen '459 requires that the entire
10   forward and backward channel be utilized to time-synchronize the mobile units. In
11   fact, a satellite-based timing system is required to keep time aligned between cells.
12   Therefore, the system disclosed by Gilhousen '459 is clearly a time-synchronous
13   CDMA cellular telephone communications system, and is not intended for, or
14   useable as, a high data-rate radio-frequency inter-computer communications system.
15   Kerr, US Patent Nos. 4,635,221 and 5,001,723, describes a system that
16   utilizes the bandwidth available in a surface-acoustic-wave convolver, which
17   generally has a much higher processing bandwidth than the bandwidth available for
18   signal transmission. A received signal is multiplexed onto several carrier frequencies,
19   and each is processed independently in the convolver. The convolver is used to
20   simultaneously compare the received signal to M orthogonal reference waveforms,
21   composed of Walsh function and PN-DSSS waveforms. The '723 patent describes
22   a variation that uses orthogonal sinusoids instead of Walsh functions, as taught by
23   the '221 patent. The scope of the teachings of these patents is narrow in that they
24   specifically address a method of demodulating a plurality of signals using a
25   convolver, and do not disclose any means for implementing a high-data-rate wireless
26   local-area-network suited for use in a multipath environment.
27   Groth, US Patent No. 4,494,238, discloses use of pseudo-noise direct-
28   sequence spread spectrum across multiple, non-contiguous carrier frequencies that
29   are coherently processed at a receiver. Walsh functions are used in this system to
30   generate signals within the receiver, such signals being used to perform phase
31   computations, but not for signaling over a communications channel corrupted by
32   multipath interference.

1   McRae et al., US Patent No. 4,872,182, provides a method for determining

2   a useful frequency band for operating a high frequency radio communications

3   network.   Each receiver is identified by its pseudonoise direct-sequence spread

4   spectrum reference code, which implies that spread spectrum encoding is used for

5   CDMA purposes, even though the term "CDMA" is not explicitly mentioned.

6   Walsh-function modulation is used to specify control information for scanning

7   available frequency bands until a useful frequency band is found.

8

9   ## Objects of the Invention

10   It is a general object of the present invention to provide a wireless LAN of

11   the type described that overcomes the problems of the prior art.

12   More specific objects of the present invention include providing a wireless

13   LAN that achieves superior data rates while providing reliable communications.

14   Another object of the invention is to overcome intersymbol and intrasymbol

15   interference resulting from multipath effects, and to thereby provide a higher data

16   rate with more robust performance than previously possible.

17   Another object of the invention is to provide a practical means for

18   implementing a high-reliability, high-data-rate, wireless local-area network.

19

20   ## Summary of the Invention

21   The invention provides an apparatus and method for providing high data rates

22   in a wireless local-area network data communications environment, even in the

23   presence of multipath interference. To achieve this, the invention combines a

24   higher-order signaling alphabet, such as an orthogonal signal set, with direct-

25   sequence spread-spectrum modulation (DSSS) to provide processing gain for

26   suppressing both intra-symbol and inter-symbol interference due to multipath effects,

27   while also providing the high rates of data throughput required of a wireless LAN.

28   Furthermore, the use of DSSS in this high data rate application reduces intrasymbol

29   interference effects to the extent that the need for diversity methods is significantly

30   diminished.

31   Use of a higher-order signalling alphabet results in a symbol waveform that

32   is $\log_2 M$ times longer than an equivalent binary signalling waveform, where M is the

1   order of the higher-order signalling alphabet. The longer-duration symbol waveforms

2   of the higher-order signalling alphabet are co-modulated with a DSSS waveform so

3   as to provide increased processing gain for a given data rate, without increasing the

4   spread spectrum transmission bandwidth. The increased processing gain results in

5   robust performance at a data rate that is sufficiently high to provide a practical

6   wireless LAN.

7   For some applications, the use of a non-orthogonal high-order signalling

8   alphabet results in acceptable performance, as measured by a low bit-error rate for

9   a given signal-to-noise ratio. Examples of non-orthogonal symbol sets include

10   quadrature amplitude modulation (QAM) signal constellations, and M-ary phase shift

11   keying sets, when transmitting more than two bits per symbol.

12   In a preferred embodiment, the higher-order alphabet that is used is mutually

13   orthogonal. The use of M-ary orthogonal signaling to implement the higher-order

14   alphabet is normally prohibited by the narrowband channel allocations available; to

15   convey n bits per symbol, the bandwidth required is M times the symbol rate, where

16   the value of M is 2^n. The fine structure (high frequency components) required to

17   support M orthogonal waveforms, as expressed by the exponential relationship

18   between n and M, leads to exponentially increasing bandwidth requirements. For

19   example, for a given symbol rate, increasing the number of bits transmitted per

20   symbol from 4 to 5 results in a 25% increase in throughput (data rate), but requires

21   a 100% increase in transmitter bandwidth.

22   An example of an orthogonal signalling set that fits within, i.e., is supported

23   by, the bandwidth of a direct sequence spreading code is the Walsh-function

24   waveform set. As a high-order alphabet, these waveforms can be directly modulated

25   by pseudo-noise spread spectrum modulation, without exceeding the occupied

26   transmit bandwidth required for spread spectrum signalling alone. Since spread

27   spectrum frequency allocations and spread spectrum transceiver equipment are

28   inherently wideband, the Walsh-function waveform set does not require additional

29   bandwidth when used in conjunction with DSSS encoding, even though it requires

30   more bandwidth than the signal to be encoded when only Walsh-function encoding

31   is used.

1   Consequently, use of the words 'spreading' and 'despreading' are to be
2   interpreted as referring to modulation and removal, respectively, of a DSSS encoding
3   waveform, whether or not there is a change in bandwidth due to the DSSS
4   waveform. In the case of a Walsh-function waveform of a bandwidth that.is less
5   than the bandwidth of the DSSS encoding waveform, the term 'spreading' and
6   'despreading' may be understood in a more conventional sense.

7   The invention employs a Walsh-function waveform set that includes a
8   plurality of mutually orthogonal binary waveforms which can be synchronously
9   modulated upon a spread spectrum code such that all binary transitions of both the
10   Walsh-function waveforms and the spread spectrum waveforms occur simultaneously
11   with a transition of a common clock signal. The clock signal frequency is selected
12   so as to support the finest possible pulse structure in each Walsh-function and spread
13   spectrum waveform. The finest pulse structure that can occur in a waveform
14   determines the bandwidth of the waveform. Therefore, the clock rate establishes the
15   bandwidth of the waveform. As long as a waveform signal transition occurs at a
16   clock edge, a multiplicative composite of a Walsh-function and spread spectrum
17   waveform will not require additional bandwidth beyond the bandwidth of its two
18   constituent waveforms. Consequently, Walsh-function waveforms having a
19   bandwidth less than or equal to the bandwidth of the DSSS waveform can be used
20   without any increase in bandwidth of the Walsh-function/DSSS composite waveform.

21   In another preferred embodiment, the orthogonal signal set is supplemented
22   with an antipodal signal set to form a bi-orthogonal signal set, further increasing the
23   data rate achievable at a given DSSS processing gain. Other embodiments include:
24   noncoherent signalling across two symbols, as in differential phase shift keying
25   (PSK), to perform the bi-orthogonal signalling; coherent and noncoherent M-ary
26   phase shift keying, combined with orthogonal signalling within a single symbol; and
27   differentially encoded coherent phase shift keying across two symbols, with
28   orthogonal signalling within a symbol.

1   <u>Brief Description of the Drawings</u>

2   The invention will be more fully understood from the following detailed

3   description, in conjunction with the accompanying figures, wherein:

4   Fig. 1 is a schematic representation of a communications channel affected by

5   multipath interference;

6   Fig. 2 is a plot of time versus the log of measured impulse response of a

7   typical short range multipath channel exhibiting both intrasymbol and intersymbol

8   interference;

9   Fig. 3 is a block diagram of a spread spectrum transmitter and time-domain

10   representations of associated waveforms;

11   Fig. 4 is a block diagram of the correlation process used in a receiver to

12   despread a line-of-sight (LOS) signal encoded by DSSS, and then corrupted by

13   communications channel interference, thermal noise, and multipath effects;

14   Figs. 5A, 5B, and 5C are, respectively, a time-domain signal plot of line-of-

15   sight and reflected signals, a block diagram, and a correlation process output plot,

16   together showing a correlation process operating on the sum of the line-of-sight and

17   reflected signals to produce a correlation process output trace;

18   Fig. 6 is a plot of time versus the log of measured impulse response showing

19   the elimination of the significant intersymbol interference provided by DSSS

20   encoding of each symbol;

21   Fig. 7 is a chart of LAN types showing rapid synchronization requirements;

22   Fig. 8 is a block diagram of a spread spectrum transmitter;

23   Fig. 9 is block diagram of a spread spectrum receiver having a rapid

24   synchronization circuit which provides a timing signal to a correlator demodulator;

25   Fig. 10 is a schematic of a spread spectrum receiver having a sliding serial

26   correlator for performing synchronization;

27   Fig. 11 is a diagram of an example of a data packet structure;

28   Fig. 12 is a schematic diagram of a correlator demodulator that employs

29   bandpass direct-sequence (DS) removal;

30   Fig. 13 is a schematic diagram of a non-phase-coherent correlator

31   demodulator for orthogonal signalling that employs baseband DS removal and

32   noncoherent DPSK;

1   Fig. 14 is a schematic diagram of a phase-coherent correlator demodulator

2   for orthogonal signalling that employs baseband DS removal and coherent PSK;

3   Figs. 15A - 15H are waveform traces showing the first eight Walsh-function

4   waveforms in ascending Walsh order;

5   Fig. 16 is a plot of the probability of correctly demodulating a 1024-bit data

6   packet versus signal-to-interference ratio for DPSK signaling and orthogonal

7   signalling at various data rates;

8   Fig. 17 is an enlarged portion of the plot of Fig. 16;

9   Fig. 18 is an integrated circuit layout diagram of a charge transfer device

10   implementation of a receiver of the invention;

11   Fig. 19 is a schematic diagram of demodulator chip circuitry for use with a

12   coherent carrier-phase reference signal;

13   Fig. 19A is block diagram detailing the add/subtract block of Fig. 19;

14   Fig. 20 is a schematic diagram of the demodulator chip circuitry for use with

15   a carrier signal of unknown phase, wherein both in-phase and quadrature-phase

16   channels are processed, and wherein the combining circuitry of the demodulator chip

17   is shown schematically;

18   Figs. 21A and 21B are schematic diagrams showing a preferred partitioning

19   of the circuitry of Fig. 20 into two chips, or for realizing a cascadeable structure;

20   Fig. 22 is a schematic diagram of a basic cell for computation of Walsh

21   coefficients; and

22   Fig. 23 is a schematic diagram of a plurality of the basic cells of Fig. 22

23   interconnected in a tree architecture, for computation of Walsh coefficients.

24

25   ## Detailed Description of the Drawings

26   The invention provides an apparatus and method for reducing multipath

27   interference effects, while also providing high data rates in a local-area network data

28   communications environment. The apparatus and method of the invention combines

29   a higher-order signaling alphabet, such as an orthogonal signal set, with direct-

30   sequence spread-spectrum (DSSS) modulation.

31   As recognized by the invention, an orthogonal signalling set that requires no

32   more bandwidth than the bandwidth of the spreading code of the DSSS modulation

1   is, for example, the set of Walsh-function waveforms. As a high-order alphabet,

2   these waveforms can be combined with a pseudonoise (PN) direct sequence spread

3   spectrum (DSSS) waveform without increasing the occupied transmit bandwidth

4   beyond the bandwidth required for the spread spectrum signalling alone. The Walsh-

5   function signal set includes binary waveforms which can be synchronously multiplied

6   by the DSSS waveform such that all binary transitions of the Walsh-function

7   waveforms occur at transitions of the same clock signal that generates the DSSS

8   waveform.

9   The bandwidth of a waveform is determined by the finest possible pulse

10   structure of the waveform. Since each clock transition represents a potential signal

11   transition, the clock rate establishes the finest possible pulse structure of a signal

12   waveform. Any signal transition of the highest bandwidth waveform that occurs at

13   a clock edge will not require additional bandwidth beyond the bandwidth of the clock

14   signal.

15   There exist other ways to provide an orthogonal signal set for use with spread

16   spectrum techniques. Instead of using a separate multiplicative orthogonal signal set,

17   such as the Walsh-functions, in conjunction with a single pseudo-noise spreading

18   code to implement the signaling, the symbol waveform can be chosen from among

19   a set of nearly orthogonal pseudo-noise (PN) spreading codes, or phase shifts of

20   these spreading codes. Modulations that transmit a variety of shifts of the same code

21   include pulse position modulation (PPM), and cyclic code shift keying, for example,

22   but these time-shift modulations are unsuitable because the demodulation can be

23   ambiguous when subjected to multipath time delays. Modulations that send one of

24   a set of PN spreading waveforms to relay the data also have several problems.

25   Only PN waveforms that are cyclic, maximal-length sequences without data

26   modulation exhibit the requisite nearly orthogonal cross-correlation properties.

27   Randomly chosen PN waveforms exhibit average cross-correlation values (between

28   different pairs of waveforms) that are equal to the processing gain of the PN

29   waveform. It is difficult to derive a subset of waveforms that have good cross-

30   correlation properties. The number of required waveforms increases exponentially

31   with the number of bits per symbol that must be transmitted. These waveforms,

1   once determined, must be generated with independent PN generators, because each

2   waveform is unrelated to each of the others in structure.

3   At the receiver, a separate spread spectrum correlator must be provided for

4   each transmitted waveform because the waveforms are generally independent of each

5   other. Each correlator operates upon the received signal, and attempts to provide

6   a level at the output of the correlator representative of the degree of correlation

7   between a received-signal waveform and a reference waveform. Each waveform that

8   can potentially be transmitted will be provided as a reference waveform in one

9   correlator. The data decision as to which waveform was actually transmitted is

10   determined by the correlator with the largest output signal.

11   By contrast, according to the invention, Walsh-functions do not exhibit these

12   problems. The regular waveform structure of the Walsh-functions allows a set of

13   waveforms of any order to be readily synthesized. In the receiver, the invention

14   exploits a decomposition property of the Walsh-function waveforms that allows a

15   correlator to be constructed from a plurality of identical elements, to be described

16   below. Thus, according to the invention, Walsh-function orthogonal data modulation

17   is the preferred form of data modulation to be used in combination with spread

18   spectrum modulation.

19   However, any means for providing the correlation against each of a plurality

20   M of Walsh-function waveforms will also suffice. Other examples, such as the fast

21   Walsh transform (also known as the fast Hadamard transform) are equally useful

22   when used in combination with spread spectrum modulation.

23   An orthogonal signal set is characterized by the property that each waveform

24   has no projection on any other waveform in the set. By contrast, an antipodal signal

25   set is characterized by the property that a waveform can have a negative projection

26   onto another waveform. By combining the two signal sets, a bi-orthogonal signal set

27   is formed, wherein both orthogonal and antipodal signals are possible. As a benefit,

28   bi-orthogonal data modulation provides an extra data bit per symbol, without

29   increasing the transmission bandwidth, or decreasing the processing gain. The

30   accompanying slight increase in required signal-to-noise ratio is insignificant.

31   A bi-orthogonal signal set can be implemented in the Walsh-function

32   demodulator, as illustrated in the exemplary embodiment of Fig. 14, wherein the

1 positive and negative phase of any of the waveforms can be used as additional

2 potential waveforms in a symbol. Thus, phase shift keying (PSK) can be combined

3 with the orthogonal signalling. Bi-orthogonal modulation can be processed coherently

4 if the phase of the received signal is tracked.

5   Alternatively, bi-orthogonal modulation can be processed non-coherently

6 using differential phase shift keying (DPSK) between symbols, as illustrated in the

7 exemplary embodiment shown in Fig. 13. If non-coherent DPSK is used, after the

8 orthogonal receiver determines which waveform was most likely transmitted for each

9 pair of consecutive symbols, the DPSK receiver determines whether it is likely that

10 there was a phase inversion between the carriers of each pair of symbol waveforms.

11 The next pair of symbols for this operation consists of the second symbol of the

12 previous pair and a new symbol, just as in binary DPSK.

13   Just as coherent PSK can be used on each symbol if a phase reference is

14 created at the receiver, multiphase phase shift keying can be used with orthogonal

15 signalling to increase data rate. However, the bit error rate performance of this type

16 of modulation degrades rapidly as the order of the signal set increases. Furthermore,

17 multilevel DPSK, such as differential quadrature phase shift keying (DQPSK) can

18 be used, which sacrifices bit error rate performance for improvements in data rate.

19   Several embodiments of the invention provide robust wireless LAN

20 performance. One such embodiment employs a different PN spreading code for each

21 successive symbol in a sequence of transmitted symbols. Errors due to high cross-

22 correlation sidelobes in multipath between transmitted symbols are thereby

23 randomized.

24   In a preferred embodiment, to further reduce error rates, error correction

25 coding can also be employed. Error correction coding can be used to compensate for

26 the portion of the error rate due to the high sidelobes that can occur under some

27 multipath delay conditions, as measured at the output of the demodulator.

28   In other embodiments, the same PN code is repeated every consecutive

29 symbol. Use of repeating PN codes can help to reduce the peak cross-correlation

30 sidelobe levels, whereas changing codes cause some randomization of the levels

31 between symbols.

1   Another embodiment of the invention uses a pulse-shaping filter on spread

2   spectrum code modulation to reduce the bandwidth required to achieve a given

3   processing gain. It is known in the art that a waveform that is square-shaped in the

4   frequency domain, i.e., having no frequency sidelobes, provides the greatest

5   processing gain. Thus, pulse shaping of the code trades higher time sidelobes for

6   lower frequency sidelobes, i.e., squareness in the frequency domain.

7

8   Multipath Environment

9   Referring to Fig. 1, it is useful to distinguish two major types of multipath

10 interference. "Near-in" multipath interference is caused by the existence of a

11 reflected version 28 of a line-of-sight (LOS) 26 signal that has travelled only a small

12 distance further than the direct line-of-sight signal 26, thereby causing coherent

13 cancellation and deep fading of the signal power of the received signal, which is a

14 combination of at least the reflected signal 28 and the LOS signal 26. This type of

15 reflected signal is delayed with respect to the LOS signal 26 no longer than the

16 duration of one data symbol of the LOS signal 26, and so the interference resulting

17 therefrom is referred to as "intra-symbol" interference. This type of multipath

18 interference results from a signal travel path that reflects off a surface such that it

19 is incident upon the receiver at a small angle with respect to the LOS signal 26.

20   Various frequency components of the LOS signal 26 and the reflected signal

21 28 destructively interfere at the receiver, resulting in nulls in the received frequency

22 spectrum. For example, if a narrowband signal, i.e, a signal occupying a relatively

23 narrow frequency range (commonly used in traditional communications) is used to

24 modulate a carrier signal of a frequency that falls within a null in the received

25 frequency spectrum, and the narrowband signal traverses both an LOS path and a

26 reflected path to a receiver, the amplitude of the received modulated signal will be

27 substantially diminished. It is even possible that the amplitude of the modulated

28 signal will be diminished to an amplitude less than the amplitude of the noise

29 introduced by the communications channel, resulting in data errors. This effect is

30 known as multipath fading.

31   For example, where a receiver is disposed at a distance of 200 meters from

32 a transmitter, and a signal reflector is disposed at a perpendicular distance of 45

1   meters from a line-of-sight path between the receiver and the transmitter, a reflected

2   signal that originates at the transmitter, and is reflected towards the receiver by the

3   reflector traverses an additional 20 m with respect to the distance traversed by a line-

4   of-sight (LOS) signal. Thus, in this example, the reflected signal arrives about 65

5   nanoseconds (ns) later than the LOS signal. If the reflection is specular, which is

6   often the case, the amplitude of the reflected signal can be nearly equal to the

7   amplitude of the LOS, thereby causing deep multipath fading.

8   "Far-out" multipath interference occurs when a reflected signal travels a

9   distance sufficiently greater than the distance traversed by the line-of-sight signal so

10   as to cause a delay greater than the duration of one data symbol. The interference

11   that results is called "intersymbol interference" (ISI). The causes of reflection can

12   be similar to the causes of reflection in "near-in" multipath, but the geometry of the

13   transceiver locations with respect to the reflecting surfaces creates an excess reflected

14   path length that can extend beyond the symbol duration before it is sufficiently

15   attenuated below the amplitude of the LOS signal. The invention removes the

16   previously existing limitation that far-out multipath interference imposed on the data

17   rate of binary communications.

18   When the reflection of the signal corresponding to a first data bit overlays the

19   direct path signal corresponding to a second data bit, intersymbol interference (ISI)

20   results. ISI can cause data recovery errors at the receiver. For example, if the

21   transceivers are separated by 200 meters, and a reflector is disposed at a

22   perpendicular distance of 150 meters from the line-of-sight path and equidistantly

23   with respect to each transceiver, there is a reflected path that is 160 meters longer

24   than the direct path traversed by the line-of-sight (LOS) signal. Thus, the reflected

25   signal arrives at a time that is about 535 ns after the arrival time of the LOS signal.

26   Binary signalling would be limited to much less than 2 Mbps in this operating

27   environment.

28   Fig. 2 shows a plot of a typical filtered impulse response measurement of a

29   wireless LAN communications channel. Here, T represents the duration of the

30   symbol. The initial (filtered) pulse represents the line-of-sight response to an

31   impulse that is transmitted. All later responses are due to reflections. Both the

32   intrasymbol and intersymbol interference are apparent for this value of T.

1   Spread Spectrum Performance Advantages

2   With reference to Fig. 3, pseudonoise direct-sequence spread spectrum

3   techniques (PN-DSSS) employ a multiplicative modulation step that distributes the

4   transmitted signal over a greater range of frequencies (bandwidth) than is normally

5   required to support the data rate. For example, binary data 30 is used to phase-shift-

6   key-modulate a carrier signal 32 in a first modulator 34. The output 36 of the first

7   modulator 34 has a frequency bandwidth that is on the order of the data rate of the

8   binary data 30. The sharp signal transition 38 in the modulating data signal 30

9   causes a phase inversion 39 of the modulated signal 36. According to Fourier

10   transform theory, the phase inversion 39 introduces high frequency signal

11   components within the signal bandwidth.

12   The finest pulse structure 40 in the PN-DSSS spreading code 42 is commonly

13   referred to as a chip 40, to distinguish it from a bit, which refers to the smallest

14   possible pulse of a data signal. The PN-DSSS spreading code 42 phase-shift-key

15   modulates the waveform 36 within a second modulator 44, resulting in many more

16   phase inversions within each data symbol of an output waveform 45. The output

17   waveform 45 of the second modulator 44 has a bandwidth that is equal to the

18   bandwidth of the PN-DSSS code. The order of application of the modulations of

19   modulators 34 and 44 can be reversed, and the modulations can also take the form

20   of minimum-shift-keying, or various other continuous-phase-shift-keying waveforms

21   that are known in the art.

22   Referring to Fig. 4, within a receiver 46, the spreading code 42 is removed

23   by a correlation process, such as can be implemented in a matched filtering or serial

24   correlator 48, using a reference code 49. The correlation process implemented by

25   the correlator 48 provides a linear decomposition 50 of the individual propagation

26   paths that make up the received signal. The decomposition is inherent in the signal

27   processing and requires no feedback. Therefore, wideband channel dynamics can be

28   handled without computational strain, in contrast with adaptive equalizer systems.

29   As depicted in Fig. 4, the correlation process 48 within the receiver 46

30   performs a cross-correlation of the local reference code 49 and the received signal

31   47 after it has been corrupted by transmission through a communications channel.

32   The correlation process output 50 is depicted for a range of relative displacements

1   of the received signal with respect to the reference code signal. The spreading code

2   signal 42 is chosen such that the amplitude of its autocorrelation function is nearly

3   zero everywhere except where the signals are aligned. Where the signals align, there

4   occurs a triangular pulse, called a correlation spike 50, of width $2/T_c$ at its base,

5   where T_c is the chip width.

6   The peak of the correlation spike 50 occurs at perfect alignment. Recall that

7   each bit of the spreading code is referred to as a chip, to distinguish it from a data

8   bit. Thus, if there are sixteen chips of spreading sequence in a cross-correlation

9   interval, e.g., the duration of a symbol, there are 16 possible ways the spreading

10   code can be aligned with respect to the signal to be correlated, when the chip edges

11   are also aligned. Fractional chip timing shifts account for unknown chip boundary

12   timing. The correlation process determines which of the relative positions results in

13   significant signal energy (correlation spike), the remaining relative positions having

14   negligible signal energy, i.e., no appreciable signal spike.

15   Referring to Fig. 5, PN-DSSS spread spectrum modulation of the reflected

16   signal 52 and the LOS signal 54 allows them to be resolved in time at the receiver

17   using the correlation process 56, thereby eliminating multipath interference. After

18   the correlation process 56, each signal 52 and 54 is represented by a displaced

19   correlation spike 52a and 54a, respectively, each spike having an amplitude which

20   represents relative received signal strength. In fact, the output of the correlation

21   process, as the relative code alignment is swept out, approximates the impulse

22   response of the communication channel resolved to the spreading bandwidth, as it

23   is the linear sum of the autocorrelation functions of all of the signal paths.

24   According to the invention, a benefit of the use of PN-DSSS spread spectrum

25   signaling is the mitigation of severe far-out multipath ISI. In a preferred

26   embodiment, this is achieved by changing the spread spectrum waveform on each

27   data symbol so that the ISI from each data symbol does not correlate with the DS

28   code on any following symbols.

29   Fig. 6 is a plot of the correlation process output for the channel impulse

30   response of Fig. 2. The far-out multipath portion of the channel impulse response

31   58 has been truncated beyond the symbol time because each data symbol is

32   modulated by a different PN-DSSS waveform.

1   The correlation process can be implemented by using a serial correlator or

2   a matched filter, or an approximation to either. A serial correlator (also called a

3   sliding correlator) tests for signal detection after a period of processing called the

4   detection interval. A detection interval is typically longer than a data symbol

5   because more signal energy is needed to detect a signal than is needed to demodulate

6   the signal to ensure acceptable wireless LAN performance.

7   The longer detection intervals are achieved by further integrating (either

8   coherently or non-coherently) over multiple coherent-integration intervals, where

9   each coherent-integration interval is of a duration normally associated with a data

10   symbol. After a detection interval, if signal detection is not achieved, the serial

11   correlator slides the reference timing by a fraction of a PN-DSSS code chip. The

12   number of detection intervals that must be checked is the determined by the

13   uncertainty in code timing and the amount of oversampling of the chip timing. For

14   example, if timing is completely unknown and the detection portion of the preamble

15   is a repeated sequence of sixteen chips, with a correlation every half chip for

16   oversampling to prevent straddling loss, then no more than thirty-two detection

17   intervals are required to achieve the proper timing for detecting a received signal.

18   If the detection interval is ten symbols long, the transmitter must send a preamble

19   that is 320 symbols long before sending any data. Furthermore, since the DSSS

20   sequence is repeated within the preamble, and detection can occur on any repetition,

21   after signal detection occurs, frame synchronization must be obtained to determine

22   which symbol is the beginning of the data stream. Since there is sufficient signal-to-

23   noise ratio for detection, frame synchronization can be accomplished using a simple

24   frame sync bit pattern structure that is easily recognized.

25   It is commonly known that a matched filter synchronizer, or an equivalent

26   device, can test all code timing relationships in a single detection interval, and

27   therefore can serve as a fast synchronizer. The matched filter synchronization will

28   be unambiguous in timing, in contrast with a serial correlator. Various

29   approximations to a full-scale matched filter include a binary-quantized-input

30   matched filter, or a matched filter that includes some non-coherent processing, or a

31   matched filter that performs the full timing search in several steps (but not to the

32   extent of a serial correlator).

1   The choice of whether to use a correlator or a matched filter for

2   synchronization depends on the application. A correlator is much less expensive and

3   less technology dependent. A matched filter is computationally intensive. A

4   correlator can be used if the application can tolerate long synchronization overheads,

5   or if there is a means to aid the detection process using a suitable data link protocol.

6

7   Local-area Network Channel Access Protocol

8   A communications-channel access protocol is a set of procedures that enables

9   multiple users to access a common communications channel. For example, in some

10   communications environments, where a plurality of transmitters use the same

11   communications frequency band, a communications-channel access protocol, based

12   upon throughput requirements and communications traffic priorities, requires that

13   each of a plurality of transmitters take turns transmitting over the channel. To send

14   large blocks of data, computer communications protocols often break the data into

15   smaller blocks called packets and send these. The packets are re-assembled at the

16   receiver. Packetizing the data allows multiple users to share the communications

17   channel fairly and efficiently.

18   Fig. 7 compares six known protocol types with respect to the speed of the

19   synchronizer circuit required. The protocol that is used affects which speed

20   synchronizer is required because synchronization overhead affects average data

21   throughput. For example, signal detection in a serial correlator synchronizer is slow,

22   in general, but its speed can be improved by using prior timing information if such

23   use is supported by the protocol. The timing information can be determined by long-

24   term tracking of timing at coarse resolution to minimize the timing uncertainty on

25   each data packet. Alternatively, the timing information can be determined by central

26   control of timing through broadcast transmissions from a timing hub. This type of

27   communication system will be referred to as "time-slotted" to suggest the

28   synchronous nature of the control information.

29   If the channel is not time-slotted, but is instead random access, then the

30   length of the data packet used is critical. If the data packets are much longer than the

31   preamble required for serial correlator synchronization, then the preamble will not

32   affect the communications channel throughput efficiency. However, if it is desirable

1   for the duration of the data packet to be short compared to the preamble, then a fast

2   synchronizer must be used to preserve channel efficiency. Short data packets are

3   sometimes required for optimizing traffic flow according to the type of data that is

4   to be transmitted, for re-transmission control, or for operating in burst-interference

5   environments.

6   It is commonly known that a matched filter synchronizer, or an equivalent

7   device, will test all code timing relationships in a single detection interval, and

8   therefore can serve as a fast synchronizer. It is essential that the synchronizer used

9   is fast enough to obtain the low synchronization overhead required when short data

10   packets are used.

11   Another approach is a network based on message-switching instead of packet

12   switching. In message switching, communications traffic is packetized, but each user

13   of the channel transmits messages, where each message includes a series of packets,

14   and no other user can interrupt a message. The synchronization does not need to re-

15   occur in each packet as it does in packet switching where each consecutive packet

16   can be transmitted by a different user. As seen in the chart of Fig. 7, only the packet

17   switched, random access protocol that uses short packets requires a fast

18   synchronizer.

19   If the transmissions are message switched, or if the packets are longer than

20   the clock stability or Doppler shift will allow, then a time-tracking loop must be used

21   to maintain synchronization throughout a transmission. As an example, assume that

22   a data rate of 5 Mbps and a packet length of 200 Kbits are used, resulting in packets

23   of 40 ms duration. If the required time alignment must be held to within 20 ns

24   (which must be substantially less than the duration of a code chip) of the initial

25   synchronization timing, then a net clock offset of 20 ppm is required between the

26   transmitter and receiver. Alternatively, a delay-locked timing control loop can be

27   used to maintain the reference code alignment with the received signal. Alternatively,

28   an automatic frequency control (AFC) loop can be used to lock the clock

29   frequencies.

30   An embodiment of the transmitter for the wireless LAN communication

31   system of the invention is shown in Fig. 8. A computer interface 60 provides a

32   stream of binary data which is first divided into a sequence of data words by a

1   symbol grouping module 62, each data word representing a symbol value. The

2   symbol values may be optionally passed through an encoder 64 for error correction

3   coding. For orthogonal signaling, Reed-Solomon error correction codes may be used

4   with symbols matched to the modulation alphabet. For bi-orthogonal signaling, Reed-

5   Solomon codes can be used exclusively, or a hybrid Reed-Solomon/binary coding

6   technique can be used wherein Reed-Solomon coding is used to correct the

7   orthogonal-demodulation process, and binary correction is used for symbol-to-symbol

8   phase-inversion demodulation.   Erasure decoding, whereby potential errors are

9   indicated in the decoder based upon, for example, amplitude information, is an

10   option with either orthogonal or bi-orthogonal signaling. For example, a symbol

11   error that arises during orthogonal demodulation would make suspect the validity of

12   a phase-inversion decision using the corresponding erroneous symbol.

13   More specifically, error correction coding commonly strives to correct a large

14   number of correctable errors within a group of symbols. The group is called a

15   "coding block". The Reed-Solomon coding block comprises a set of the original data

16   symbols concatenated with some "check" symbols that appear the same as the data

17   symbols but actually contain the coding information. As more check symbols are

18   included with the data, more data symbols which are in error can be corrected. The

19   ratio of data symbols to the total group size is called the "coding" rate. For example,

20   "rate 1/2" coding means there are an equal number of data symbols and check

21   symbols. Rate 1/2 is considered a low rate code. As a result of low-rate coding, the

22   minimum signal-to-noise ratio in a Gaussian noise environment that the demodulation

23   can effectively operate upon is reduced, and tolerance to bursts of errors can be

24   achieved.

25   The apparatus and method of the present invention can use coding for a

26   somewhat different purpose, and thus an aspect of the present invention is to include

27   a coding approach that is generally considered unsuitable for the more common

28   coding applications, such as for satellite communications or for correcting errors on

29   hard disk drives used in computers. Those applications generally require low rate

30   codes and large coding blocks to achieve the desired performance. In fact, there are

31   integrated circuits available that implement the common coding approaches and they

32   were found to be unsuitable for this application. As a unique problem of the wireless

-24-

1   data communications system based on direct sequence and Walsh orthogonal

2   signaling, depending on the direct sequence code being used and the actual multipath

3   delay, there can be an irreducible error rate that results from multipath self-

4   interference. This means that errors appear in the demodulated data even at very

5   high signal to noise ratios.

6   To solve this problem, a high rate code is used. That is, a small number of

7   check symbols per data block is preferably employed. This unique way to use coding

8   eliminates the irreducible error rate while maintaining the high throughput

9   requirements of the wireless data communications network. If the more common

10   coding approach were used, the irreducible errors would be eliminated, but at the

11   cost of a severe drop in data throughput, and a severe increase in hardware and

12   software complexity. According to an aspect of the present invention, while such

13   costs are often deemed necessary for other applications, it is not desirable for solving

14   the multipath problem in the wireless data communications network.

15   The high rate error correcting code may be aided by changing the direct

16   sequence code on each symbol, which randomizes the effect of the multipath on each

17   symbol, even though the multipath is static between symbols. Furthermore, a short

18   coding block is preferably used. The short coding block allows the high rate code

19   to provide robust packet performance even with a small amount of correctibility

20   within each block. There are other reasons that the smaller coding block is

21   desireable: a smaller library of direct sequence codes may be used from which codes

22   are selected for changing on each symbol within a block; less latency occurs between

23   the demodulator and the computer; there are less computational requirements, and

24   less data storage is used while the correction is invoked.

25   For applications which must be tolerant to bursts of errors, only a large

26   coding block can be used. For random errors, on the other hand, a given code rate,

27   and hence tolerance to some average error rate, may be achieved by different block

28   sizes as long as the ratio of check symbols to block symbols is the same. Because

29   longer code blocks offer somewhat better performance, conventional coding designs

30   normally employ long blocks. The term "short block" as used herein means a block

31   size small enough that a given average random error rate may be tolerated with only

32   the ability to correct a single error. While conventional coding implementations must

1   employ complex, iterative decoding procedures running in sophisticated processors,

2   single-error-correcting codes may be decoded directly using relatively modest digital

3   logic. Thus, the use of a short coding block allows high-data-rate error correction

4   with low delay and simple circuitry.

5   As a preferred embodiment, the high rate code is a single-error-correcting

6   Reed-Solomon code whereby only one symbol in each coding block may be

7   corrected. Thus a simple implementation of a decoder may be built that uses a

8   simple symbol wide feedback shift register or a look-up table containing the entire

9   decoding operation when the encoded signal is received, as described in greater

10 detail, hereinafter. A coding block that is 15 symbols long with 2 check symbols

11 forms a single-error-correcting Reed-Solomon coding block that is rate 13/15 (also

12 written as RS(15,13)), which can handle symbol-error rates approaching 1/15, and

13 which can be decoded at the receiver within a minimal time period and with a

14 minimum of computational complexity.

15   The basic RS(15,13) code is used for just the Walsh-Orthogonal part of the

16 signaling (with either coherent or noncoherent demodulation). For Walsh-Bi-

17 Orthogonal signaling (coherent or noncoherent demodulation) it is necessary to

18 provide for correction of the binary element of the data in addition to the Reed

19 Solomon coding. At the symbol signal-to-noise ratios required for orthogonal

20 modulation, errors in the binary portion of the waveform are several orders of

21 magnitude less probable than orthogonal-signaling errors, and hence, can be

22 tolerated. If occasionally a transmitted packet of data is lost due to a random binary

23 bit error, this will occur, on the average, much less frequently than packets being

24 lost due to too many orthogonal-signaling errors (more than a single orthogonal error

25 in a 15-symbol block using RS(15,13)).

26   The effect, on binary signaling, of having made an orthogonal-signaling

27 error, however, is not negligible because the orthogonal demodulation is used to

28 select the processing channel upon which to perform the binary portion of the

29 demodulation. For coherent bi-orthogonal, for example, the occurence of an error

30 in the orthogonal waveform decision will cause a 50% probability of error for the

31 corresponding binary bit. On the other hand, for noncoherent bi-orthogonal

32 signaling, the occurence of an orthogonal-signaling error will cause a 50%

1   probability of error on the two DPSK bits which use that complex amplitude in

2   forming a DPSK decision. Fortunately, the strong correlation between orthogonal-

3   signaling errors and binary errors makes erasure decoding attractive, and erasure

4   decoding requires fewer check bits than for random error correction.

5   As a specific case, the preferred coding for Walsh-Bi-Orthogonal signaling

6   with 5 bits per symbol employs a 15-symbol block with 13 5-bit information

7   symbols. The two 5-bit check symbols provide for correction when an arbitrary 4-bit

8   orthogonal demodulation error occurs. After the R-S FEC has located and corrected

9   the 4-bit orthogonal-signaling error, then the location of the suspected pair of DPSK

10   bits, likely to be in error, is known. The binary (fifth) bits for each of the 5-bit

11   check symbols conveys, respectively, parity for the even and odd sets of binary bits

12   demodulated. This means that the adjacent binary DPSK bits are checked by

13   different parity bits which makes parity checking useful for DPSK in which errors

14   are likely to appear in pairs. Because random binary errors can be ignored, it is

15   assumed that a single error can occur in either binary data group (even or odd) and

16   the location of the binary bit that is suspect is known when an orthogonal-signaling

17   error has been made. Hence the pair of parity bits is sufficient to correct the binary

18   data.

19   Referring again to Fig. 8, the data modulator 66 translates its input data into

20   corresponding Walsh function symbol waveforms, and an appropriate phase change

21   is then optionally added between symbols. The data modulator 66 translates its input

22   symbol value into corresponding Walsh-function symbol waveforms by selecting

23   from either a stored set of waveforms, or by selecting corresponding logic in a

24   digital waveform generator. For the bi-orthogonal or differentially bi-orthogonal

25   modulation, the phase inversion control is accomplished by either complementing or

26   not complementing the binary Walsh-function output so as to increase the

27   information content of the symbols, thereby increasing the data rate. An exclusive

28   OR logic gate 72 then combines the resultant waveform with a PN-DSSS waveform

29   69 generated by a direct sequence pseudonoise generator 70. The output of the logic

30   gate 72 drives an RF modulator 74 that provides a transmit signal 76, which is then

31   amplified by an RF amplifier 78 for broadcast over an antenna 80 as packets of data.

1   The order of application of the modulations provided by the modules 70, 72,

2   and 74 are unimportant, and can therefore be reversed. Also, the RF modulator 74

3   can be implemented in stages, for example, by first employing intermediate

4   frequency modulation, then employing modulation with a final transmitted frequency,

5   with associated filtering.

6   The data modulator 66 can incorporate any phase shift modulation, in addition

7   to the selection of the Walsh function. Coherent M-ary PSK, or non-coherent

8   differential phase shifts between symbols, such as DPSK, DQPSK, or differential M-

9   ary PSK, can be used to increase data rate when signal-to-noise ratio is sufficiently

10   high. Appropriate error correction encoding can be used in conjunction with these

11   modulation schemes.

12   With reference to Fig. 9, in one embodiment of the invention, a receiver 84

13   includes a rapid synchronizer 82. The output of the rapid synchronizer 82 controls

14   the timing of the combination Walsh-function and PN correlator 86 and the PN

15   reference generator 83. Various implementations of a Walsh-function/direct sequence

16   correlator, such as the Walsh-function/pseudonoise correlator 86 of Figs. 9 and 10

17   are provided in Figs. 12, 13, and 14. Schemes for fast synchronization are well-

18   known in the art, and can be used in a variety of forms with this invention. One-

19   example is a matched filter. Another example is an aided-acquisition correlator. The

20   rapid synchronizer 82 must include a detection circuit with a detection threshold

21   level. The threshold level may be fixed or it may be determined as a function of

22   received signal level.

23   The correlator 86 drives a demodulator 88 that performs a maximum

24   likelihood decision, or an approximation thereof. The correlator 86 has a plurality

25   M of outputs, the number M of outputs being equal to the order M of the M-ary

26   signal 85 to be demodulated. The particular output of the M outputs having the

27   largest magnitude will most likely correspond to the reference waveform that

28   matches the waveform that was transmitted. Accordingly, the M outputs of the

29   correlator 86 drive the demodulator 88, which selects the largest magnitude output

30   from among all the correlator 86 outputs.

31   Any phase shift data modulation that is used in addition to orthogonal

32   modulation can be ideally demodulated by correlating against all possible waveforms

-28-

1   in the demodulator 88. Alternatively, phase shift keying (coherent or noncoherent,

2   and within a symbol or between symbols) can be demodulated separately by

3   operating the demodulator 88 only on the selected orthogonal values resulting in

4   insignificant loss in performance.

5   In an exemplary embodiment, for DPSK combined with M-ary orthogonal

6   signalling, the M-ary orthogonal waveforms in each symbol pair are first

7   demodulated. The outputs of the correlators that contained the largest outputs on

8   successive symbols would then be used in the DPSK demodulation. In another

9   exemplary embodiment, for coherent PSK combined with M-ary orthogonal

10   signalling, the M-ary orthogonal waveforms in each symbol are first demodulated.

11   The output of the correlator that contained the largest output for each symbol would

12   then be compared to a phase reference in the PSK demodulator.

13   In the demodulator 88, after demodulation is performed, each demodulated

14   symbol is then decoded for errors, if error correction coding was employed in the

15   transmitter. The decoded symbols 89 are then concatenated within the data interface

16   92 to form a binary data stream to be received by a computer.

17   Note that no delay-locked timing control loop is included, because it is

18   assumed that the packets are short enough to require rapid synchronization.

19   However, a delay-locked loop or an AFC loop can be included if the packets are

20   nevertheless too long for the timing drift specification, or if a variable length packet

21   is desired.

22   With reference to Fig. 10, an embodiment of a receiver of the invention is

23   shown that uses correlator synchronization, and includes an optional delay-locked

24   time-tracking control loop 90. Any of the Walsh waveforms can be used as a

25   synchronization signal transmitted at the start of a packet. As an illustrative example,

26   the lowest order waveform W_0 will be used. In this case, the correlator 86 performs

27   a serial correlator search for the PN code timing, using timing information as an

28   input from a timing control module 87. The output signal W_0 is detected by a

29   comparator 93, which can be analog or digital, depending upon the implementation

30   technology of the correlator 86. The output signal of the comparator 93 is received

31   by a synchronization detector 95. The synchronization detector 95 then prevents

32   further searching for a signal and enables the demodulation process.

1   In an exemplary embodiment, the second input 94 to the comparator 93 is

2   determined by the threshold estimation module 98 that sums the respective

3   magnitudes of the outputs of one or more of the other channels 96. Since these

4   channels 96 are performing orthogonal correlation with respect to the synchronization

5   signal that is transmitted, the channels 96 provide a measure of the noise and

6   interference power in the receiver. In the absence of noise and interference, only one

7   of the channels 96 would be active. However, some degree of noise and interference

8   is inevitable, and therefore each of the channels 96 is active to some extent.

9   Combining a number of these channels 96 allows noncoherent averaging of the noise

10   and interference power of the received signal, thereby providing a detection

11   threshold level that adapts to maintain a nearly constant false alarm rate, where a

12   false alarm is an erroneous interpretation of noise or interference as a true

13   correlation signal. Using simultaneous correlations in orthogonal channels to

14   establish the detection threshold level is superior to methods which average the level

15   of a single correlator over a period that straddles multiple output samples because

16   such methods experience transient response problems.

17   The demodulator 88 of Fig. 10 is the same as the demodulator shown in Fig.

18.   9. Note that the optional time-tracking function 90, used to maintain synchronization

19   during long packets, is explicitly indicated in Fig. 10, whereas the time-tracking

20   function is implicit in Fig. 9. Methods for implementing the time tracking module

21   90 are well-known and include early/late correlation and time dither, and also

22   include AFC if the source of timing drift is clock offset or Doppler.

23   An example of a data packet structure 100 that can be used with the invention

24   is shown in Fig. 11. The data packet structure 100 includes a header portion 101,

25   a data portion 102, and a trailer portion 103. The header portion 101 includes a

26   preamble 104, a source address 106, a destination address 108, and a packet length

27   110. The preamble includes the synchronization signal, and optionally includes

28   signals that the receiver can use to verify that a detection event occurred. The length

29   of the preamble 104 is determined by the type of synchronization used. The

30   preamble 104 can also be followed by other control information, such as error

31   correction type or error checking on the control information itself. The body of the

32   packet holds the data 102. The trailer 103 includes a cyclic redundancy check code

1   112 for final error detection. The trailer can also include acknowledgment

2   information 114 regarding the successful or unsuccessful receipt of previous packets;

3   this is known as "piggybacked" acknowledgements.

4   Figs. 12, 13, and 14 show details of the combined Walsh-function and PN

5   correlator block 86, and the data demodulator block 88 of Figs. 9 and 10. For

6   purpose of illustration only, these examples will use an 8-ary Walsh modulation to

7   provide 3 bits per symbol. However, it should be recognized that the same circuits

8   can be applied to orthogonal signaling of an arbitrary number of bits per symbol,

9   including binary orthogonal signaling.

10   Pseudonoise (PN) removal can be performed directly on an intermediate

11   frequency, or on the transmission frequency, by at least one mixer 115 and at least

12   one bandpass filter 116, as shown in Fig. 12. If the Walsh-function coding does not

13   occupy the full spread spectrum bandwidth (i.e., if there is more than one PN chip

14   per Walsh-function clock cycle), then the bandpass filter 116 can filter to the Walsh-

15   function bandwidth, resulting in a partial correlation. In this case, the bandpass

16   filter 116, which can be implemented as a surface acoustic wave (SAW) filter,

17   provides a square-shaped impulse response that filters the input waveform so that it

18   falls within the bandwidth of the Walsh-function modulation. This filtered signal 117

19   is then split and sampled in I and Q channels by respective mixers 118, low pass

20   filters 120, and A/D converters 122 thereby forming a complex representation of the

21   signal 117, the I channel representing the real component, and the Q channel

22   representing the imaginary component of the signal 117. The output of the A/D

23   converters 122 is received by the Walsh-function demodulators 124 that correlate the

24   signals with a reference Walsh functions. The outputs of the correlators 124 are

25   envelope demodulated in a combining circuit 126 that provides an envelope output

26   for each set of the eight sets of complex (I and Q) channels for the 8-ary modulation.

27   The eight envelope outputs are compared in a 8-way comparator 130 to provide a

28   largest magnitude index indicating which complex correlator 124 yielded an envelope

29   output having the largest magnitude. The largest magnitude index indicates the most

30   likely data symbol transmitted, as determined by the linear correlation process

31   performed in the correlators 124. The data decoder 132 receives the largest

32   magnitude index and the eight envelope outputs, and performs either a direct

1 decoding to a binary stream of the selected Walsh-function correlator envelope

2 output, or performs an optional Reed-Solomon, or hybrid Reed-Solomon and binary

3 code error decoding if bi-orthogonal signalling is also used.

4   Fig. 13 shows and exemplary embodiment wherein PN removal is performed

5 after analog-to-digital conversion, and immediately prior to performing Walsh-

6 function correlation. It is also possible to perform PN removal at baseband using an

7 analog multiplication prior to A/D conversion (not shown). The demodulator can be

8 the same as the demodulator 130, 132 used Fig. 12, or DPSK can optionally be

9 added between symbols. This form of signalling is called the non-coherent bi-

10 orthogonal signalling, because DPSK is used.

11   To perform the DPSK demodulation, the output 152 of the 8-way magnitude

12 comparison module 150, which module determines the largest correlator output, is

13 used in selector 146 to multiplex to its output, from among the 8 complex amplitudes

14 145, the complex amplitude 147 of the largest signal, which complex amplitude 147

15 is to be used in the DPSK demodulation.

16   The DPSK decision is made using the selected outputs of two successive

17 symbols in the complex multiplier 158 by using a symbol delay 154, taking the inner

18 product of the largest amplitude correlator outputs and deciding the sign of the

19 result. Independently, the index of the largest of each symbol is saved in a symbol

20 delay module 156 as the correct value of the Walsh-function signaling. The data

21 decoder 160 receives the Walsh demodulation result from the symbol delay

22 module 156 and the DPSK demodulation result from the complex multiplier 158.

23 These results are combined in the data decoder 160 by concatenating the single-bit

24 DPSK answer with the 3-bit Walsh-correlator answer to obtain a 4-bit output (16-ary

25 alphabet) on each symbol. Optionally, the data decoder 160 applies an error

26 correction algorithm. The data decoder 160 then converts each resulting symbol into

27 an equivalent binary data sequence for processing by a computer (not shown). The

28 data decoder 160 serves to invert the operations performed by modules 62, 64, and

29 66 in Fig. 8. Note that symbol delay 156 is optional in accordance with which

30 particular symbol aligns with the transmitted DPSK modulation. With symbol delay

31 module 156 in place, the DPSK result aligns in the data decoder 160 with the Walsh-

1   function symbol that was transmitted during the leading symbol of the DPSK symbol

2   pair.

3   Fig. 14 shows a single channel demodulator for use with a coherent phase

4   reference signal 164. An IF signal 166 is filtered by a bandpass filter 168. The

5   filtered IF signal is multiplied by the coherent phase reference signal 164, which is

6   provided by a carrier recovery loop (not shown). The resulting signal is low pass

7   filtered by a low pass filter 170, and is then converted to a digital signal by an

8   analog-to-digital converter 172. The resulting digital signal is despread by a PN

9   correlator 176 using the PN reference code 174, and the resulting despread signal

10   is then Walsh-function demodulated in a Walsh correlator 178. Any of the above

11   described techniques for PN removal and Walsh-function demodulation can be

12   applied, and can be applied in any order. If the PN spreading code is a higher rate

13   modulation than the Walsh modulation, then the despread PN can be collapsed to the

14   Walsh bandwidth in the PN correlator 176. Because the phase reference signal 164

15   is used, only a single channel (channel I) is required in this correlator. A sign

16   stripping module 180 strips the sign bit from the digital signal provided by the walsh

17   correlator 178, and an 8-way compare module 182 determines which correlator

18   output of the correlator 178 is the largest. Since the phase reference signal 164

19   preserves coherence, optional PSK modulation can be used to provide coherent bi-

20   orthogonal signalling. Demodulation requires that the sign bit of the largest value be

21   selected in the sign register 184. A data decoder 186 optionally performs error

22   detection and correction, and disassembles the symbol groups of the signal provided

23   by the 8-way compare module 182 into a binary data stream for processing by a

24   computer (not shown).

25

26   Walsh-Function Signaling

27   The first eight Walsh functions are shown in Figs. 15A-15H. The lowest

28   order Walsh function is shown in Fig. 15A, and the other Walsh functions are shown

29   in ascending order in Figs. 15B-15H. The lowest order function is referred to as W_0.

30   Since in a communications environment the Walsh functions are a function of time,

31   the Walsh functions may also be represented as $W(n,t)$ or $WAL(n,t)$, where n is the

32   order of the particular Walsh function, and t represents time.

1   The Walsh functions are digital waveforms each being mutually orthogonal

2   with respect another Walsh waveform of different order when multiplied therewith,

3   i.e., the integral of the product of any two Walsh functions of different order being

4   equal to zero. The order of each Walsh function is equal to the number of binary

5   transitions exhibited by the function. For example, WAL(0,t) does not have a binary

6   transition, whereas WAL(2,t) has two binary transitions. Equivalently, the Walsh

7   function waveforms can be viewed as having one or more binary states over the

8   duration of the waveform, wherein a binary state can be of a duration no greater

9   than a minimum duration, called a Walsh chip.

10   For each symbol of a message, one of these digital waveforms can be

11   logically combined by an exclusive-or logic gate with a direct-sequence spread

12   spectrum code to create another digital waveform that can be used to phase modulate

13   a carrier that has been modulated by the message.

14   Fig. 16 shows four probability curves. A curve denoted by DPSK shows the

15   probability of correctly demodulating a 1024-bit packet of data using DPSK spread-

16   spectrum signaling as a function of normalized signal-to-interference (S/I) in decibels

17   (db). Three additional curves, denoted by the data rates (in bits per symbol) 8 b/s,

18   4 b/s, and 2 b/s, show the probability of correctly demodulating a 1024-bit packet

19   of data using M-ary orthogonal signalling with 8, 4, and 2 bits per symbol,

20   respectively. It must be stressed that M-ary orthogonal signaling is a form of coding;

21   if the DPSK modulation were combined with coding, it would also shift to a lower

22   required signal-to-interference ratio.

23   Fig. 17 shows the same curves on an expanded scale. Note that the use of 4-

24   ary orthogonal (2 bits/symbol) is substantially equivalent to DPSK, and that a higher

25   signaling alphabet (4 b/s or 8 b/s) significantly improves performance. For an

26   uncoded link, the above curves imply that, for a given bandwidth, the S/I ratio that

27   can be tolerated at the receiver by combining M-ary (M > 2) orthogonal signaling

28   with PN-DSSS spread spectrum is larger than the S/I ratio that can be tolerated by

29   combining PN-DSSS spread spectrum and either binary (M = 2) signalling or

30   DPSK. Conversely, for example, a transmission using 4 bits/symbol and a PN-

31   DSSS bandwidth of 80 Mhz can tolerate as much interference at the receiver as a

32   transmission using DPSK and a direct-sequence bandwidth of about 130 Mhz!

1   A rotation of the PN-DSSS code, known as cyclic code-shift keying (CCSK),

2   provides an orthogonal set with some of the advantages of using the Walsh functions,

3   such as the property that the bandwidth required for orthogonal signaling can equal

4   the direct-sequence bandwidth, without further expansion of the signal bandwidth

5   over that of the PN-DSSS code. Use of CCSK results in a correlator output

6   waveform that is pulse-position modulated (PPM). However, in a multipath

7   environment, the PPM-like behavior of CCSK can be problematic because an

8   important feature of the signal, the delay discriminant used for demodulation, can

9   be incorrectly interpreted as multipath. Thus, the use of CCSK is not preferable to

10   the use of Walsh functions in a multipath environment.

11   If the bandwidth expansion due to the orthogonal signaling is much smaller

12   than the direct-sequence spreading, then any orthogonal set can be used; in this case

13   a convenient choice is a set of tones (i.e., M-ary FSK) which is demodulated using

14   a fast Fourier Transform (FFT) technique after the spreading code is stripped off.

15   However, when the spreading due to the orthogonal signaling approaches that due

16   to the DSSS modulation, the actual transmission bandwidth depends upon both the

17   direct sequence and orthogonal modulation since the pair of modulations cannot be

18   synchronously superimposed in any way because they are drastically dissimilar

19   modulations.

20   Even though both CCSK and Walsh functions have the property that the

21   bandwidth required for orthogonal signaling can equal the direct-sequence bandwidth,

22   without further expansion of the signal bandwidth over that of the PN-DSSS, CCSK

23   cannot be used effectively in a multipath environment. Thus, for the purpose of

24   limiting bandwidth and enhancing performance in a multipath environment, the

25   Walsh functions are preferable to CCSK.

26

27   Walsh Function Correlation Processor

28   For this discussion, assume a received signal has been modulated using both

29   PN-DSSS and Walsh functions. Also assume that, in the receiver, the reference PN-

30   DSSS code for demodulating the received signal is properly aligned with the received

31   signal, where synchronization is achieved by using, for example, a matched filter or

32   a time-sliding serial correlator. Further, assume that the received signal and the

1   local reference signal are multiplied together to form a despread signal, and that the

2   despread signal is then low-pass filtered to facilitate processing the highest-order

3   Walsh function. (For example, the highest-order Walsh function can have a

4   bandwidth that only includes frequencies that are less than the DSSS chip rate.) The

5   despreading operation has the effect of removing the PN-DSSS code, leaving only

6   the Walsh function modulation.

7.   The discussion below considers in-phase baseband processing. In an actual

8   implementation, since carrier phase is usually unknown, the signal is converted to

9   in-phase and quadrature channels, and the in-phase processing described below is

10   performed in each channel, followed by envelope combining of the corresponding

11   amplitudes before data decision.

12   One way to obtain the required correlations in the Walsh function correlation

13   processor (e.g., modules 86, 124, 144, 178) is to implement a fully parallel fast

14   Walsh transform. This approach becomes attractive only as the order of the Walsh

15   functions becomes large. A preferred method for executing a fast Walsh transform

16   is to exploit the mathematical structure of the Walsh functions by computing the

17   Walsh function coefficients using a plurality of basic cells, shown in Fig. 22,

18   interconnected as a tree structure having successive stages, as shown in Fig. 23. The

19   clock rate of each successive stage is reduced by half with respect to the previous

20   stage, and each successive stage has twice the number of cells, thereby keeping the

21   computation rate per stage the same at each stage. The power consumed per stage,

22   mostly dependent on computation rate, is therefore also nearly constant.

23   Furthermore, the number of computation elements is far fewer than the number

24   required in the fully parallel fast Walsh transform.

25   The parallel fast Walsh transform requires $M(\log M)$ computation elements

26   per M-ary output. By contrast, the tree structure shown in Fig. 23 uses $2(M - 1)$

27   computation elements per M-ary output. Therefore, at larger values of M, the tree

28   structure of Fig. 23 is superior to the parallel architecture (not shown) for calculating

29   the Walsh transform, because the number of computation elements per M-ary output

30   is significantly less in the case of the tree structure. Both structures perform the

31   same number of computations per symbol. The tree structure provides an tradeoff

1   that is advantageous when implementing it as an integrated circuit, in that quantity

2   of hardware can be traded for hardware operation rate.

3   Referring to Fig. 22, a basic cell 250 accepts input samples serially at input

4   252 at a rate f_{in}, and generates two output samples in parallel at outputs 254 and 256

5   at a rate $f_{in}/2$. Thus, a serial pair of input samples forms a parallel pair of output

6   samples. One output sample of the output pair is the sum of a current pair of serial

7   input samples, and the other sample of the output pair is the difference of these two

8   input samples.

9   Fig. 23 shows a tree 252 of basic cells 250 for decoding the first eight Walsh

10   functions W_0 - W_8. Note that through the application of arithmetic sums and

11   differences, each path through the tree represents a multiplication of the input

12   sequence by a specific combination of (binary) square-wave functions and summing

13   the result. In fact, the specific square-wave function for each path is a product of

14   Rademacher functions, whose products are known to generate the Walsh functions.

15   Also note that the tree structure naturally conserves power because each

16   successive stage includes twice the number of elements as the previous stage, but

17   runs at only half the clock rate of the previous stage. Further, layout of the design

18   on an integrated circuit is simplified, because the higher fanout signal distributions

19   operate at proportionally lower rates. Therefore, slower circuits are connected by

20   longer signal routes, as is desirable in an integrated circuit.

21   The Walsh function correlation processor can be implemented using a field

22   programmable gate array, although the detailed implementation technique is not

23   relevant. Field programmable gate array implementations are facilitated by the tree

24   structure because the higher fanout routes of such an implementation, being longer,

25   can operate more slowly. Alternatively, the processor can be implemented entirely

26   in software executed by a digital signal processing microprocessor. For high

27   bandwidths, the processor can be efficiently implemented using a charge-transfer

28   device (CTD).

29

30   Charge-Transfer Device Implementation

31   Charge-transfer devices (CTD) include charge-coupled devices (CCD),

32   acoustic-charge-transfer (ACT) devices, and bucket-brigade devices (BBD). Each of

1   these technologies represent signals as electronic charge, and process the signals by

2   manipulating electronic charge. CTD technologies can perform both synchronization

3   and demodulation. A CTD can take discrete-time analog samples at its input,

4   perform all the signal processing, and provide the resulting digital data decisions at

5   its output. Since the CTD input is a capacitive storage cell, the analog signal is

6   inherently sampled as the CTD input is clocked. This operation is similar to the

7   sampling capacitor in a sample and hold circuit.

8   Alternatively, a digital approach requires high speed D/A converters that are

9   costly. By contrast, the input linearity of a CTD supports far more processing gain

10   than is needed for this application, at sampling rates of 50 Msps for CCD devices

11   to 360 Msps for ACT devices. These sampling rates include a factor-of-two

12   oversampling, relative to the signal bandwidth, to prevent excessive straddling loss.

13   Higher sampling rates are possible by operating two devices in parallel and

14   staggering the clocks. The signal can be processed with analog precision against the

15   binary digital reference signal.

16   A Walsh demodulator can be configured using a CTD 190, as shown

17   schematically in an exemplary embodiment in Fig. 18. The electrical input to a CCD

18   190 is connected to signal charge injection wire 191 which is bonded to the surface

19   of the substrate at input electrode 192. A clock signal on the clocking electrodes 195

20   transfers the sampled charge packet serially along the row of charge storage cells

21   193. After each clock period, during which period, each charge storage cell receives

22   the charge packet previously stored in the charge storage cell to its left, the signal

23   sensing electrodes 194 read the level of charge stored in each cell.

24   Alternatively, in an ACT, signal samples are handled similarly, but the

25   clocking electrodes of the CCD are replaced by the electric potential of a traveling

26   surface acoustic wave. In a BBD, the clocking of signal charge is effected via

27   clocked pass transistors, but the signal treatment is analogous.

28   A Walsh demodulator requires sample delays for providing storage of

29   waveform samples, as is provided in the charge storage cell 193 that is within the

30   substrate beneath the clocking electrodes 195, and beneath the signal sensing

31. electrodes 194. Walsh combination circuits 198 perform Walsh correlations on

32   signals provided by the signal sensing electrodes 194, thereby providing a plurality

1   of envelope outputs. Then, a magnitude circuit and M-way compare circuit 200

2   provide a largest magnitude index signal 201 indicating which correlator of the

3   Walsh combination circuits 198 yielded an envelope output having the largest

4   magnitude. The largest magnitude index signal 201 is provided to a detect/data

5   decode circuit 202 which performs data demodulation upon the signal.

6   If the PN-DSSS code is of a higher bandwidth than the CTD can support, the

7   bandwidth of the received signal can be reduced before being processed by the CTD

8   by removing the PN-DSSS modulation in a pre-correlator, after DS chip timing has

9   been established during the synchronization cycle. The CTD can then performing

10 Walsh correlations, data demodulation, and data decoding.

11   Establishing synchronization can also be performed in the CTD, either by a

12 reconfiguration of the demodulation CTD channels, or by a separate CTD channel

13 operating in parallel. If the same chip rate is preferred for both synchronization and

14 demodulation, and if the preferred chip rate is higher than 25 MHz (for a 50 Msps

15 device), parallel CCDs may be used, combined with a multiplexing structure to

16 implement a matched filter.

17   Alternatively, the ACT technology could be used because of its higher

18 inherent sampling rates. As another alternative, since there is no baud rate

19 requirement for synchronization, a longer symbol can be used with a lower PN-

20 DSSS code rate, thereby preserving processing gain.

21   The number of code chips in the matched filter can be further increased so

22 as to provide a robust synchronization preamble. Precise timing can then be achieved

23 in a sequential operation. In this way, for example, a spread spectrum code rate of

24 25 Mhz can be used for synchronization, while a Walsh chip rate of 25 Mhz can be

25 used to encode data modulated by a 75 Mhz spread spectrum code that can be

26 removed in the pre-correlator.

27   An important advantage of CTDs is that all associated support circuits and

28 the storage cells can be integrated on the same device. Since modern CCDs use

29 storage that resembles a dynamic RAM, CCD technology has benefitted directly

30 from advances in packing density and speed of DRAM technology.

31   The magnitude and 8-way compare circuit 200 and the detection and data

32 decode circuit 202, (and optionally timing and frequency control loops), for example,

1   are integratable directly on the device output, thereby greatly simplifying output

2   processing.

3

4   Digital Implementation

5   The chip architecture is based on the basic cell and tree structure of Figs. 22

6   and 23. This architecture is efficiently achieved as in an integrated circuit (IC) or as

7   a field programmable gate array (FPGA), since it is register-intensive and tree-like

8   in form. A benefit of the tree architecture is that, even thought each stage includes

9   the twice the amount of circuitry as its preceding stage, the later stage is only

10 required to operate at half the speed of its preceding stage. The power distribution

11 on the chip is thereby evenly distributed, and routing requirements of the most

12 speed-intensive circuits are reduced. Consequently, the higher-speed input stages can

13 use optimized routing. Also, the last stage, which operates relatively slowly and

14 which requires many routing channels due to having the highest adder fanout, can

15 be placed without constraint.

16   Communication over a non-Gaussian communications channel requires that

17 a digital signal processor receive a wider input word than communication over a

18 Gaussian communications channel. In a Gaussian channel, good signal normalization

19 can be used to reduce the number of bits per input word to as low as one, thereby

20 providing substantial hardware savings.

21   With reference to Fig. 19, to accommodate non-Gaussian interference, and

22 to reduce the accuracy required of the signal normalization circuits (e.g., automatic

23 gain control), the embodiment of Fig. 19 uses 6 bit per word input samples 206 (5

24 bits plus a sign bit). A series of clock signal dividers 205 provides progressively

25 slower clock signals. The input samples 206 are clocked into an input register 207.

26 The first stage add/sub module 208, shown in detail in Fig. 19A, operates on the

27 six-bit two's-complement input 209 with sign extension to produce a seven bit output

28 211.

29   To support 10 Mbps 8-ary signalling, the add/sub block 208 must operate at

30 a 26.67 MHz clock rate. This is because a symbol rate of 3.333 Msps (million

31 symbols per second) is required with eight Walsh chips/symbol (for 8-ary

32 modulation) to achieve 10 Mbps with 3 bits/symbol.

1   Referring to Fig. 9A, clock signal A is twice the speed of clock signal B,

2   having been divided by a factor of two by a clock signal divider 205. Consequently,

3   an adder 210A and a subtractor 210B operate in parallel to provide a pair of outputs

4   at a rate that is half the rate that input samples are presented to the add/subtract

5   module 208.

6

7   Clocking

8   After a pair of input samples are loaded into an input register 208A of the

9   first add/subtract module 208, the results of adding and subtracting operations

10   performed by modules 210A and 210B, respectively, are latched out upon the arrival

11   of the next input sample. Thus, even though the add/subtract module 208 operates

12   on a pair of samples at a time, the result must be ready in a single sample time.

13   Similarly, the second stage Add/Sub blocks 212 operate on a pair of output samples

14   211 of the first stage Add/Sub block 208. The results must be latched out to the

15   next stage before next input samples arrive.

16   The third stage add/subtract modules 214 have been modified so that the

17   output register 216 is placed after the 8-way compare 218, thereby eliminating an

18   extra frame delay, as well as eliminating M-1 registers (where M = 8, in this

19   example). The third stage add/subtract modules 214, and the 8-way compare circuit

20   218, operates at one fourth the input rate. If double buffering were used at the input

21   to each stage, the computation rates would be halved, because an extra set of

22   samples would be stored while awaiting processing.

23   There is typically some skew (delay) between the arrival of the clock signals

24   at the latches of the inputs and the outputs of each stage. The difference between

25   the latest arrival time of the input clock to the earliest arrival of the output clock, if

26   positive, must be added to the maximum delay path of the logic to determine

27   clocking rate. Excess delay may be added to the output clock to increase the speed,

28   provided care is taken that minimum hold times are met for the shortest possible

29   logic delay path.

30   The 8-way compare circuitry 218 is shown as an inverted binary tree

31   structure having one half as many elements in each successive stage as in a previous

32   stage. Since a single receiver channel is shown, the coherent carrier reference case

1   is assumed, as shown in Fig. 14. Thus, envelope detection is just a sign stripping

2   function. First, the magnitude of each nine-bit envelope signal from the add/subtract

3   modules 214 is determined in the sign-strip modules 220.   Then, magnitude

4   comparisons are performed in pairwise fashion at each stage resulting in a single

5   magnitude, of the largest byte, from a winning correlator. The value of the largest

6   byte of each comparison is passed along to the next stage, while the index of the

7   corresponding correlator is interpreted by the 7-to-3 decoder 222 as the orthogonal

8   data demodulation result.

9

10   Architecture for full I and Q processing

11   In Fig. 20, the pipelined architecture described in Fig. 19 is duplicated for

12   the Q channel, wherein the circuitry for the I and Q channels are combined, with the

13   8-way compare circuitry, to provide full I and Q processing. Fig. 20 shows how

14   quadrature-channel combining is performed, using the well-known approximation of

15   adding the output of the largest value of the I 230 or Q 231 channels on each output

16   pair to one half the output of the smaller value, in the combine I and Q blocks 232.

17   Therefore, the sign stripping, as performed by a sign strip module 220, is still

18   necessary on each channel.

19   According to the invention, the circuitry of Fig. 20 can be partitioned so as

20   to provide a plurality of identical or nearly identical integrated circuits, the integrated

21   circuits each being a cascadable structure suitable for combining with similar

22   integrated circuits to form M-ary Walsh demodulators of arbitrary values of M.

23   The most direct way of accomplishing this partitioning, such that it becomes

24   possible to partition the circuitry of Fig. 20 into FPGA chips, or into multiple

25   custom or semicustom integrated circuits, is to place a single Walsh correlator on

26   each chip. Additionally, the I and Q combining circuits are placed on a third chip

27   that also includes 8-way compare circuitry. This approach to partitioning requires

28   that each Walsh correlator chip include 64 output lines (8 bits by 8 channels), and

29   that the combiner chip include 128 input lines. This amount of I/O is excessive,

30   resulting in high cost and reduced reliability.

31   Referring to Figs. 21A and 21B, the partitioning approach taught by the

32   invention is to divide the circuitry into an upper segment 240, shown in Fig. 21A,

1   and a lower segment 242, shown in Fig. 21B, keeping the I channel 244 and Q

2   channel 246 of each segment together on the same chip. The upper and lower

3   segments 240 and 242 are not connected until after the final comparison of the

4   comparison tree 248. The upper segment circuits 240 can be placed on one chip, and

5   the lower segment circuits 242 can be placed on another chip. Only twenty four data

6   lines are required to connect the two chips.

7   In the 8-ary circuitry shown in Figs. 21A and 21B, after the first stage, seven

8   lines in each of the I and Q channels are for interfacing to the other chip, and four

9   complex correlators (244, 246) are included on a chip. The four I and four Q

10   correlators (244, 246) on each chip are identical to those in Fig. 20, but relate to

11   only half the tree structure shown in Fig. 20. After the four I and Q results are

12   combined on each chip, they are reduced to a single largest value in a 4-way

13   compare module 248. This largest value (an 8-bit amplitude), along with two

14   decoding lines, is exported to the other chip where it is compared to the result from

15   the other half of the comparison tree, whereupon the largest of the two values is

16   decoded. The result is a three bit word representing a demodulated symbol.

17   The circuitry may be further subdivided by parsing each section 240, 242

18   similarly into two smaller chips. Similarly, the chips may be cascaded in the case of

19   higher order alphabets, i.e, higher values of M. It is also possible to form a more

20   symmetric partitioning by having one chip serve as a front-end source that feeds

21   individual segments of the tree. For improved operating speed, necessary for higher

22   alphabets, the number of signal lines between chips can be traded against speed of

23   a speed-optimized front end. The symmetric front-end source is obtained by splitting

24   the first stage Add/Sub block with the sum output feeding the upper segment and the

25   difference output feeding the lower segment. A single input line can determine

26   whether that stage is an adder or subtractor.

27   This approach allows use of multiple FPGA technology chips, or the use of

28   multiple custom or semicustom integrated circuits, while maintaining modest size and

29   interconnect complexity in each chip to increase yield and reliability. This approach

30   allows a single chip of common circuits to be cascaded vertically and horizontally

31   by a user to create arbitrarily large alphabets.

1   Other modifications and implementations will occur to those skilled in the art

2   without departing from the spirit and the scope of the invention as claimed.

3   Accordingly, the above description is not intended to limit the invention except as

4   indicated in the following claims.

What is claimed is:

1. 1.   An apparatus for communicating data between at least two data
2. devices, the apparatus comprising:
3.   means for acquiring data from a data device;
4.   means for representing the data as a sequence of digital waveform symbols,
5. the digital waveform symbols being selected from a set that includes more than two
6. unique digital waveform symbols, each digital waveform symbol being characterized
7. by a symbol duration;
8.   means for generating a direct-sequence spread spectrum encoding signal;
9.   multiplying means for combining the direct-sequence spread spectrum
10. encoding signal with the sequence of digital waveform symbols to provide a transmit
11. signal;
12.   modulator means for modulating a carrier signal in accordance with the
13. transmit signal to provide a modulated signal; and
14.   means for transmitting the modulated signal.

1. 2.   The apparatus of claim 1, wherein the direct-sequence spread spectrum
2. encoding signal is a pseudonoise direct-sequence spread spectrum encoding signal.

1. 3.   The apparatus of claim 1, wherein each of the unique digital waveform
2. symbols is orthogonal with respect to each other unique digital waveform symbol in
3. the set.

1. 4.   The apparatus of claim 3, further including means for applying
2. differential multiphase phase shift keying to each pair of sequentially neighboring
3. symbol waveforms so as to produce a waveform modulated by a combination of
4. differential M-ary PSK and M-ary orthogonal function modulation.

1. 5.   The apparatus of claim 4, wherein the means for applying differential
2. multiphase phase shift keying includes means for applying differential bi-phase shift
3. keying.

1   6.   The apparatus of claim 4, further including means for applying Reed-
2 Solomon error correction coding to each symbol waveform, and means for applying
3 binary error correction coding to the differential multiphase shift keying.

1   7.   The apparatus of claim 6, wherein said means for representing the
2 data represents said data in at least one coding block and said Reed-Solomon coding
3 includes means for correcting only a single error in a coding block and binary coding
4 comprising seperate parity bits applied to even and the odd groups of a differential
5 bi-phase shift keying data.

1   8.   The apparatus of claim 3, further including means for applying
2 multiphase phase shift keying to each symbol waveform so as to produce a waveform
3 modulated by a combination of M-ary PSK and M-ary orthogonal function
4 modulation.

1   9.   The apparatus of claim 8, wherein the means for applying multiphase
2 phase shift keying includes means for applying antipodal bi-phase phase shift keying.

1   10.   The apparatus of claim 8, further including means for applying Reed-
2 Solomon error correction coding to each symbol waveform, and means for applying
3 binary error correction coding to the multiphase phase shift keying.

1   11.   The apparatus of claim 1, wherein the set of digital waveform symbols
2 includes Walsh-function waveforms.

1   12.   The apparatus of claim 11, wherein the chip rate of the Walsh-function
2 waveforms is substantially equal to the chip rate of the direct-sequence spread
3 spectrum encoding signal.

1   13.   The apparatus of claim 11, further including means for applying Reed-
2 Solomon error correction coding to each Walsh-function waveform.

1   14.   The apparatus of claim 13, wherein said means for representing the

2   data represents said data in at least one coding block, and said Reed-Solomon coding

3   includes means for correcting only a single error in a coding block.

1   15.   The apparatus of claim 14, further including means for using a coding

2   block that is short enough such that the single error correcting will correct a

3   sufficient number of errors in a data packet that the packet failure rate will meet

4   system specifications.

1   16.   The apparatus of claim 1, wherein the multiplying means includes

2   means for synchronously multiplying the sequence of digital waveform symbols and

3   the pseudo-noise direct-sequence spread spectrum encoding signal so as to ensure

4   that the transmit signal is characterized by a bandwidth no greater than the

5   bandwidth of the pseudonoise direct-sequence spread spectrum encoding signal.

1   17.   The apparatus of claim 1, wherein the pseudonoise direct-sequence

2   spread spectrum encoding signal is periodic, and the encoding signal has a code

3   period that is longer than the symbol duration of each digital waveform symbol.

1   18.   The apparatus of claim 1, wherein the means for representing the data

2   as a sequence of digital waveform symbols includes:

3   means for grouping the data into a sequence of groups of M bits each, each

4   group representing a symbol selected from 2^M possible data symbols; and

5   data modulation means for representing each data symbol as a digital

6   waveform symbol so as to form the sequence of digital waveform symbols.

1   19.   The apparatus of claim 1, wherein the means for representing the data

2   as a sequence of digital waveform symbols further includes:

3   error correction encoding means, responsive to the means for grouping, for

4   providing error-correction-encoded data symbols.

1   20.   The apparatus of claim 1, further including a time-domain

2   pulse-shaping filter, responsive to the multiplying means, for providing the

3   transmitted signal such that the transmit signal has substantially square frequency

4   domain characteristics.

1   21.   Apparatus for receiving data communicated as a modulated signal

2   between at least two data devices, the modulated signal being of the type encoded

3   with direct-sequence spread spectrum encoding, and including digital waveform

4   symbols selected from a set of possible digital waveform symbols, the apparatus

5   comprising:

6   means for receiving the modulated signal to provide an incoming signal;

7   means for providing a timing signal;

8   despreading/correlation means, responsive to the timing signal and to the

9   incoming signal, for both removing the pseudonoise direct-sequence spread spectrum

10   encoding from the incoming signal, and for correlating the incoming signal with each

11   digital waveform symbol of a set of possible digital waveform symbols so as to

12   provide a plurality of despread correlation signals;

13   most-likely symbol means for receiving the plurality·of despread correlation

14   signals, and determining therefrom a most-likely transmitted digital waveform

15   symbol so as to provide a sequence of received symbols;

16   means for converting the most-likely transmitted digital waveform symbol

17   into a digital data sequence so as to provide a digital data stream; and

18   means for providing the digital data stream to a data device.

1   22.   The apparatus of claim 21, wherein the modulated signal is of the type

2   encoded with pseudonoise direct-sequence spread spectrum encoding, and the

3 · despreading/correlation means includes means for removing a pseudonoise direct-

4   sequence spread spectrum encoding from the incoming signal.

1   23.   The apparatus of claim 21, wherein the means for providing a timing

2   signal includes means for synchronizing to the incoming signal so as to provide the

3   timing signal in synchronization with the incoming signal.

1   24.   The apparatus of claim 23, wherein the means for synchronizing to

2   the incoming signal includes a matched filter synchronizer.

1   25.   The apparatus of claim 23, wherein the means for synchronizing to

2   the incoming signal includes a serial-correlator-based synchronizer with means for

3   accepting timing information as an input.

1   26.   The apparatus of claim 21, wherein each digital waveform symbol in

2   the set of possible digital waveform symbols is orthogonal with respect to each other

3   digital waveform symbol in the set.

1   27.   The apparatus of claim 21, wherein the set of possible digital

2   waveform symbols includes Walsh-function waveforms.

1   28.   The apparatus of claim 27, wherein the despreading/correlation means

2   includes:

3   means for direct-sequence despreading of a DSSS encoded signal so as to

4   provide a despread signal;

5   means for bandpass filtering the despread signal so as to provide a filtered

6   signal having a bandwidth substantially similar to the bandwidth of the set of Walsh-

7   function waveforms;

8   means for splitting the filtered signal into an in-phase signal and a quadrature

9   signal;

10   means for converting the in-phase signal and the quadrature signal

11   respectively into a digital in-phase signal and a digital quadrature signal;

12   Walsh-function demodulator means for correlating each digital signal with a

13   Walsh-function waveform so as to provide a Walsh in-phase signal and a Walsh

14   quadrature signal; and

15   means for envelope demodulating the Walsh in-phase signal and the Walsh

16   quadrature signal so as to provide a plurality of envelope signals,

17   wherein the most-likely symbol means includes:

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18   means for comparing each signal of the plurality of envelope signals so as to

19   determine the largest magnitude envelope signal indicating a Walsh-function

20   waveform most likely to have been transmitted, and for providing a largest

21   magnitude index signal indicative of the largest magnitude envelope signal, and

22   wherein the means for converting includes:

23   data decoder means for decoding the largest magnitude envelope signal so as

24   to provide a binary data stream.

1   29.   The apparatus of claim 28, wherein said data stream includes at least

2   one data block, and said apparatus further includes means for using a Reed-Solomon

3   error correction for correcting only a single error in a coding block.

1   30.   The apparatus of claim 28, wherein the despreading/correlation means

2   further includes means for providing a largest complex amplitude signal, the most-

3   likely symbol means further includes means for providing a largest magnitude index

4   signal, and the apparatus further comprises:

5   means, responsive to the largest complex amplitude signal and to the largest

6   magnitude index signal, for binary DPSK demodulating the sequence of received

7   symbols.

1   31.   The apparatus of claim 30, wherein the apparatus further includes:

2   means for Reed-Solomon error correction decoding and means for binary

error decoding.

1   32.   The apparatus of claim 31, wherein said data stream includes at least

2   one data block, and said apparatus further includes means for using a Reed-Solomon

3   error correction for correcting only a single error in a coding block and erasure

4   decoding of the binary stream.

1   33.   The apparatus of claim 32, whererin the erasure decoding includes

2   means for using seperate parity bits applied to the even and the odd groups of a

3   differential bi-phase shift keying data for the correction.

1   34.   The apparatus of claim 28, wherein the despreading/correlation means

2   also provides a largest complex amplitude signal, the most-likely symbol means

3   further includes means for providing a largest magnitude index signal, and the

4   apparatus further comprises:

5   means, responsive to the largest complex amplitude signal and to the largest

6   magnitude index signal, for M-ary DPSK demodulation of the sequence of received

7   symbols.

1   35.   The apparatus of claim 34, wherein the apparatus further includes:

2   means for error correction decoding.

1   36.   The apparatus of claim 27, wherein the despreading/correlation means

2   includes:

3   means for bandpass filtering the incoming signal so as to provide a filtered

4   signal having a bandwidth substantially similar to the bandwidth of the set of Walsh-

5   function waveforms with DSSS encoding;

6   means for splitting the filtered signal into an in-phase signal and a quadrature

7   signal;

8   means for converting the in-phase signal and the quadrature signal

9   respectively into an in-phase digital signal and a quadrature digital signal;

10   means for direct-sequence despreading each digital signal and correlating each

11   digital signal with a Walsh-function waveform so as to provide a despread Walsh in-

12   phase signal and a despread Walsh quadrature signal; and

13   means for envelope demodulating the despread Walsh in-phase signal and the

14   despread Walsh quadrature signal so as to provide a plurality of envelope signals,

15   wherein the most-likely symbol means includes:

16   means for comparing each signal of the plurality of envelope signals so as to

17   determine the largest magnitude envelope signal indicating a Walsh-function

18   waveform most likely to have been transmitted, and for providing a largest

19   magnitude index signal indicative of the largest magnitude envelope signal, and

20   wherein the means for converting includes:

21   data decoder means for decoding the largest magnitude envelope signal so as

22   to provide a binary data stream.

1   37.   The apparatus of claim 36, wherein the despreading/correlation means

2   further includes means for providing a largest complex amplitude signal, the most-

3   likely symbol means further includes means for providing a largest magnitude index

4   signal, and the apparatus further comprises:

5   means, responsive to the largest complex amplitude signal and to the largest

6   magnitude index signal, for binary DPSK demodulating the sequence of received

7   symbols.

1   38.   The apparatus of claim 37 ,wherein the apparatus further includes:

2   means for Reed-Solomon error correction decoding and means for binary

3   error decoding.

1   39.   The apparatus of claim 38, wherein said data stream includes at least

2   one data block, and said apparatus further includes means for using a Reed-Solomon

3   error correction for correcting only a single error in a coding block and erasure

4   decoding of the binary stream.

1   40.   The apparatus of claim 39, wherein the erasure decoding includes

2   means for using seperate parity bits applied to the even and the odd groups of a

3   differential bi-phase shift keying data for the correction.

1   41.   The apparatus of claim 36, wherein the despreading/correlation means

2   also provides a largest complex amplitude signal, the most-likely symbol means

3   further includes means for providing a largest magnitude index signal, and the

4   apparatus further comprises:

5   means, responsive to the largest complex amplitude signal and to the largest

6   magnitude index signal, for M-ary DPSK demodulation of the sequence of received

7   symbols.

1   42.   The apparatus of claim 41, wherein the apparatus further includes:

2   means for error correction decoding.

1   43.   The apparatus of claim 27, wherein the despreading/correlation means

2   includes:

3   a Walsh-function correlator, for receiving an input sample sequence, the

4   correlator including a plurality of basic cells, each basic cell having an input and two

5   outputs, the cells being interconnected to form a binary tree structure such that each

6   possible path through the tree structure represents a unique function upon the input

7   sequence, thereby providing a plurality of output sample sequences.

1   44.   The apparatus of claim 43, wherein each the basic cell accepts the

2   input sample sequence serially at a first rate f_{in}, and generates first and second output

3   sample sequences in parallel at a second rate $f_{in}/2$, such that the first output sample

4   sequence includes the sum of a current serial pair of input samples of the input

5   sample sequence, and the second output sample sequence includes the difference of

6   the current serial pair of input samples of the input sample sequence, wherein each

7   output sample sequence can be provided as an input sample sequence to another basic

8   cell.

1   45.   The apparatus of claim 43, wherein the tree structure is partitioned

2   into a plurality of circuit segments for fabrication as a plurality of individual

3   integrated circuit chips,

4   wherein each circuit segment includes an in-phase channel and a quadrature

5   channel of at least a subset of the set of Walsh-function correlators disposed on the

6   same integrated circuit chip, and

7   wherein each integrated circuit chip includes means for receiving output

8   signals from a plurality of chips so as to perform a full set of Walsh-function

9   correlations, thereby demodulating the received modulated signal.

1   46.   The apparatus of claim 27, wherein the despreading/correlation means

2   includes:

3   means for pseudonoise despreading of a DSSS encoded signal so as to provide

4   a despread signal;

5   means for bandpass filtering the despread signal so as to provide a filtered

6   signal having a bandwidth substantially similar to the bandwidth of the set of Walsh-

7   function waveforms;

8   means for heterodyning to baseband the filtered signal with a coherent phase

9   reference signal so as to provide an in-phase signal;

10   means for converting the in-phase signal into a digital in-phase signal;

11   Walsh-function demodulator means for correlating the digital signal with a

12   Walsh-function waveform so as to provide a Walsh in-phase signal; and

13   means for envelope demodulating the Walsh in-phase signal so as to provide

14   a plurality of envelope signals,

15   wherein the most-likely symbol means includes:

16   means for comparing each signal of the plurality of envelope signals so as to

17   determine the largest magnitude envelope signal indicating a Walsh-function

18   waveform most likely to have been transmitted, and for providing a largest

19   magnitude index signal indicative of the largest magnitude envelope signal, and

20   wherein·the means for converting includes:

21   data decoder means for decoding the largest magnitude envelope signal so as

22   to provide a binary data stream.

1   47.   The apparatus of claim 46, the apparatus further comprising:

2   means, responsive to the largest magnitude envelope signal and to the largest

3   magnitude index signal, for M-ary PSK demodulating the sequence of received

4   symbols.

1   48.   The apparatus of claim 47, further including means, responsive to the

2   most-likely symbol means, for performing error correction decoding on the most-

3   likely symbol if the most-likely symbol has been error-correction-encoded.

1   49.   The apparatus of claim 46, the apparatus further comprising:

2   means, responsive to the largest magnitude envelope signal and to the largest

3   magnitude index signal, for binary PSK demodulating the sequence of received

4   symbols.

1   50.   The apparatus of claim 49, wherein the means for converting the

2   most-likely transmitted digital waveform symbol into a digital data sequence includes

3   means for Reed-Solomon error correction decoding and means for binary error

4   decoding.

1   51.   The apparatus of claim 27, wherein the despreading/correlation means

2   includes:

3   means for bandpass filtering the incoming signal so as to provide a filtered

4   signal having a bandwidth substantially similar to the bandwidth of the set of Walsh-

5   function waveforms with DSSS encoding;

6   means for heterodyning to baseband the filtered signal with a coherent phase

7   reference signal so as to provide an in-phase signal;

8   means for converting the in-phase signal into an in-phase digital signal;

9.   means for direct-sequence despreading the digital signal and correlating the

10   digital signal with a Walsh-function waveform so as to provide a despread Walsh in-

11   phase signal; and

12   means for envelope demodulating the despread Walsh in-phase signal so as

13   to provide a plurality of envelope signals,

14   wherein the most-likely symbol means includes:

15   means for comparing each signal of the plurality of envelope signals so as to

16   determine the largest magnitude envelope signal indicating a Walsh-function

17   waveform most likely to have been transmitted, and for providing a largest

18   magnitude index signal indicative of the largest magnitude envelope signal, and

19   wherein the means for converting includes:

20   data decoder means for decoding the largest magnitude envelope signal so as

21   to provide a binary data stream.

1   52.   The apparatus of claim 51, the apparatus further comprising:

2   means, responsive to the largest magnitude envelope signal and to the largest

3   magnitude index signal, for binary PSK demodulating the sequence of received

4   symbols.

1   53.   The apparatus of claim 52, wherein the means for converting the

2   most-likely transmitted digital waveform symbol into a digital data sequence includes

3   means for Reed-Solomon error correction decoding and means for binary error

      decoding.

1   54.   The apparatus of claim 51, the apparatus further comprising:

2   means, responsive to the largest magnitude envelope signal and to the largest

3   magnitude index signal, for M-ary PSK demodulating the sequence of received

4   symbols.

1   55.   The apparatus of claim 54, further including means, responsive to the

2   most-likely symbol means, for performing error correction decoding on the most-

3   likely symbol if the most-likely symbol has been error-correction-encoded.

1   56.   The apparatus of claim 21, further including means, responsive to the

2   most-likely symbol means, for performing error correction decoding on the most-

3   likely symbol if the most-likely symbol has been error-correction-encoded.

1   57.   The apparatus of claim 21, including a sliding serial-correlator-based

2   synchronizer, having a signal detector, and being responsive to one of the plurality

3   of despread correlation signals, for detecting the presence of the input signal.

1   58.   The apparatus of claim 57, wherein the serial-correlator-based

2   synchronizer further includes a threshold estimator, responsive to a plurality of

3   despread correlation signals, for providing to the signal detector a signal

4   representative of an estimate of the non-coherent power of the input signal.

1   59.   The apparatus of claim 57, further including a time-tracking loop,

2   responsive to the most-likely symbol means, for extracting changes in timing

3   information from at least one signal selected by the most-likely symbol means.

1   60.   The apparatus of claim 21, wherein the most-likely symbol means

2   includes an M-way comparator having a plurality of two-way comparators

3   interconnected as an inverted binary tree structure, each two-way comparator being

4   adapted to provide an output amplitude that is the larger of two input amplitudes, and

5   for providing an index of the larger of the two input amplitudes, the M-way

6   comparator being adapted to provide an index indicating the largest of M input

7   amplitudes, and to provide the largest amplitude of the M input amplitudes.

1   61.   The apparatus of claim 60, wherein the inverted binary tree structure

2   is partitioned into a plurality of circuit segments for fabrication as a plurality of

3   individual integrated circuit chips,

4   wherein each circuit segment includes an in-phase channel and a quadrature

5   channel of at least a subset of the set of Walsh-function correlators disposed on the

6   same integrated circuit chip, and

7   wherein each integrated circuit chip includes means for receiving output

8   signals from a plurality of chips so as to perform a full set of Walsh-function

9   correlations, thereby demodulating the received modulated signal.

1   62.   The apparatus of claim 21, wherein the apparatus includes a plurality

2   of charge transfer devices.

1   63.   A method of communicating data between at least two data devices,

2   the method comprising the steps of:

3   acquiring data from a data device;

4   representing the data as a sequence of digital waveform symbols, the digital

5   waveform symbols being selected from a set that includes more than two unique

6   digital waveform symbols, each digital waveform symbol being characterized by a

7   symbol duration;

8   generating a direct-sequence spread spectrum encoding signal;

9   combining the direct-sequence spread spectrum encoding signal with the

10   sequence of digital waveform symbols to provide a transmit signal;

11   modulating a carrier signal in accordance with the transmit signal to provide

12   a modulated signal; and

13   transmitting the modulated signal.

1   64.   The method of claim 63, wherein the direct-sequence spread spectrum

2   encoding signal is a pseudonoise direct-sequence spread spectrum encoding signal.

1   65.   The method of claim 63, wherein each of the unique digital waveform

2   symbols is orthogonal with respect to each other unique digital waveform symbol in

3   the set.

1   66.   The method of claim 65, further including the step of:

2   applying differential multiphase phase shift keying to each pair of sequentially

3   neighboring symbol waveforms so as to produce a waveform modulated by a

4   combination of M-ary DPSK and M-ary orthogonal function modulation.

1   67.   The method of claim 66, wherein the step of applying differential

2   multiphase phase shift keying includes the step of applying antipodal bi-phase phase

3   shift keying.

1   68.   The method of claim 63, wherein the set of digital waveform symbols

2   includes Walsh-function waveforms.

1   69.   The method of claim 68, wherein the chip rate of the Walsh-function

2   waveforms is substantially equal to the chip rate of the direct-sequence spread

3   spectrum encoding signal.

1   70.   The method of claim 63, wherein the step of combining includes the

2   steps of:

3   synchronously multiplying the sequence of digital waveform symbols and the

4   pseudo-noise direct-sequence spread spectrum encoding signal so as to ensure that

5   the transmit signal is characterized by a bandwidth no greater than the bandwidth of

6   the pseudonoise direct-sequence spread spectrum encoding signal.

1   71.   The method of claim 63, wherein the pseudonoise direct-sequence

2   spread spectrum encoding signal is periodic, and the encoding signal has a code

3   period that is longer than the symbol duration of each digital waveform symbol.

1   72.   The method of claim 63, wherein the step of representing the data as

2   a sequence of digital waveform symbols includes the step of:

3   grouping the data into a sequence of groups of M bits each, each group

4   representing a symbol selected from 2^M possible data symbols; and

5   representing each data symbol as a digital waveform symbol so as to form the

6   sequence of digital waveform symbols.

1   73.   A method of receiving data communicated as a modulated signal

2   between at least two data devices, the modulated signal being of the type encoded

3   with direct-sequence spread spectrum encoding, and including digital waveform

4   symbols selected from a set of possible digital waveform symbols, the method

5   comprising the steps of:

6   receiving the modulated signal to provide an incoming signal;

7   providing a timing signal;

8   removing the pseudonoise direct-sequence spread spectrum encoding from the

9   incoming signal;

10   correlating the incoming signal with each digital waveform symbol of a set

11   of possible digital waveform symbols so as to provide a plurality of despread

12   correlation signals;

13   receiving the plurality of despread correlation signals, and determining

14   therefrom a most-likely transmitted digital waveform symbol so as to provide a

15   sequence of received symbols;

16   converting the most-likely transmitted digital waveform symbol into a digital

17   data sequence so as to provide a digital data stream; and

18   providing the digital data stream to a data device.

1   74.   The method of claim 73, wherein the modulated signal is of the type

2   encoded with pseudonoise direct-sequence spread spectrum encoding, and the step

3   of removing includes the step of removing a pseudonoise direct-sequence spread

4   spectrum encoding from the incoming signal.

1   75.   The method of claim 74 wherein the step of providing a timing signal

2   includes:

3   synchronizing to the incoming signal so as to provide the timing signal in

4   synchronization with the incoming signal.

1   76.   The method of claim 75, wherein the step of synchronizing to the

2   incoming signal includes:

3   using matched-filter synchronization.

1   77.   The method of claim 75, wherein the step of synchronizing to the

2   incoming signal includes:

3   using serial-correlator synchronization and accepting timing information as

4   an input.

1   78.   The method of claim 73, wherein each digital waveform symbol in the

2   set of possible digital waveform symbols is orthogonal with respect to each other

3   digital waveform symbol in the set.

1   79.   The method of claim 73 wherein the set of possible digital waveform

2   symbols includes Walsh-function waveforms.

1   80.   The method of claim 79, wherein the step of removing includes the

2   steps of:

3   direct-sequence despreading of a DSSS encoded signal so as to provide a

4   despread signal;

5   bandpass filtering the despread signal so as to provide a filtered signal having

6   a bandwidth substantially similar to the bandwidth of the set of Walsh-function

7   waveforms;

8   splitting the filtered signal into an in-phase signal and a quadrature signal; and

9   converting the in-phase signal and the quadrature signal respectively into a

10   digital in-phase signal and a digital quadrature signal,

11   wherein the step of correlating includes the steps of:

12   correlating each digital signal with a Walsh-function waveform so as to

13   provide a Walsh in-phase signal and a Walsh quadrature signal; and

14   envelope demodulating the Walsh in-phase signal and the Walsh quadrature

15   signal so as to provide a plurality of envelope signals,

16   wherein the step of receiving the plurality of despread correlation signals and

17   determining therefrom a most-likely transmitted digital waveform symbol includes

18   the steps of:

19   comparing each signal of the plurality of envelope signals so as to determine

20   the largest magnitude envelope signal indicating a Walsh-function waveform most

21   likely to have been transmitted; and

22   providing a largest magnitude index signal indicative of the largest magnitude

23   envelope signal,

24   and wherein the step of converting includes the step of:

25   decoding the largest magnitude envelope signal so as to provide a binary data

26   stream.

1   81.   The method of claim 80, further comprising the step of:

2   M-ary DPSK demodulating the sequence of received symbols.

1   82.   The method of claim 79, wherein the step of removing includes the

2   steps of:

3   bandpass filtering the incoming so as to provide a filtered signal having a

4   bandwidth substantially similar to the bandwidth of the set of Walsh-function

5   waveforms with DSSS encoding;

6   splitting the filtered signal into an in-phase signal and a quadrature signal;

7   converting the in-phase signal and the quadrature signal respectively into a

8   digital in-phase signal and a digital quadrature signal; and

9   direct-sequence despreading each digital signal so as to provide a despread

10   in-phase digital signal and a despread quadrature digital signal,

11   wherein the step of correlating includes the steps of:

12   correlating each digital signal with a Walsh-function waveform so as to

13   provide a Walsh in-phase signal and a Walsh quadrature signal; and

14   envelope demodulating the Walsh in-phase signal and the Walsh quadrature

15   signal

16   so as to provide a plurality of envelope signals,

17   wherein the step of receiving the plurality of despread correlation signals and

18   determining therefrom a most-likely transmitted digital waveform symbol includes

19   the steps of:

20   comparing each signal of the plurality of envelope signals so as to determine

21   the largest magnitude envelope signal indicating a Walsh-function waveform most

22   likely to have been transmitted; and

23   providing a largest magnitude index signal indicative of the largest magnitude

24   envelope signal,

25   and wherein the step of converting includes the step of:

26   decoding the largest magnitude envelope signal so as to provide a binary data

27   stream.

1   83.   The method of claim 82, further comprising the step of:

2   M-ary DPSK demodulating the sequence of received symbols.

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FIG. 1

FIG. 2

FIG. 4

1 / 16

DATA

MODULATOR
34

CARRIER
32

MODULATOR
44

SPREADING CODE

OUTPUT
WAVEFORM
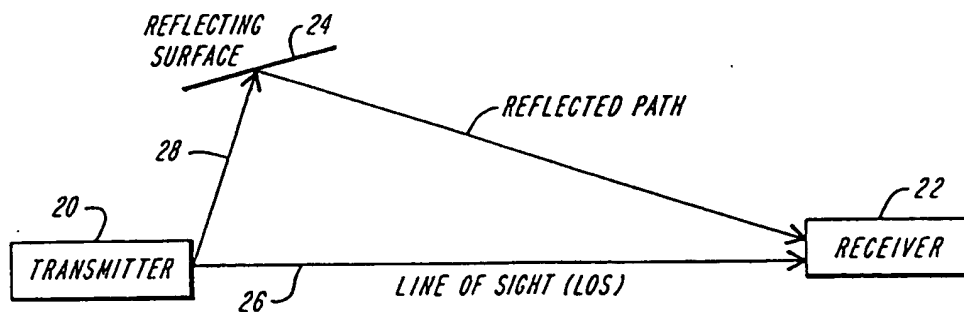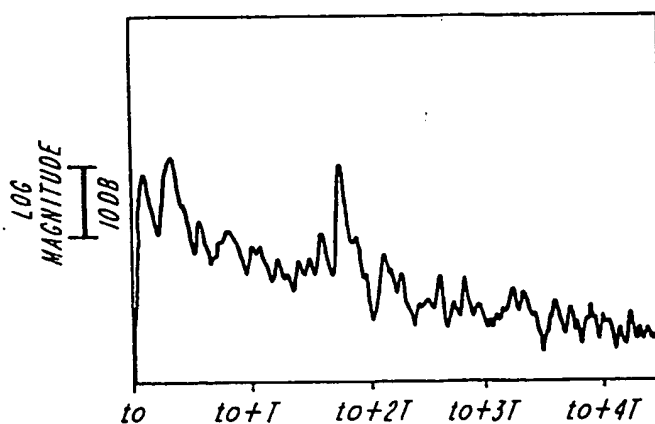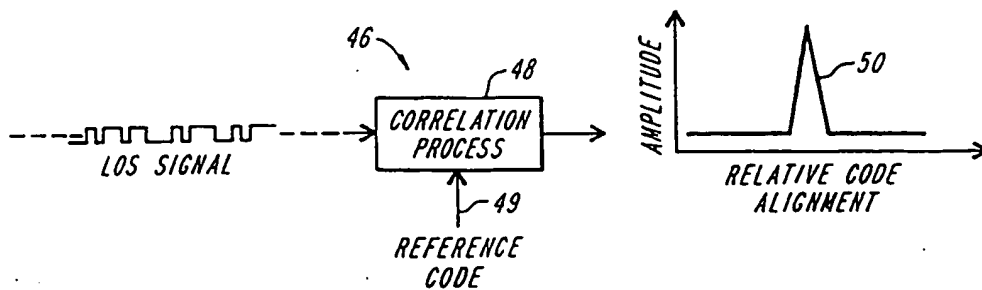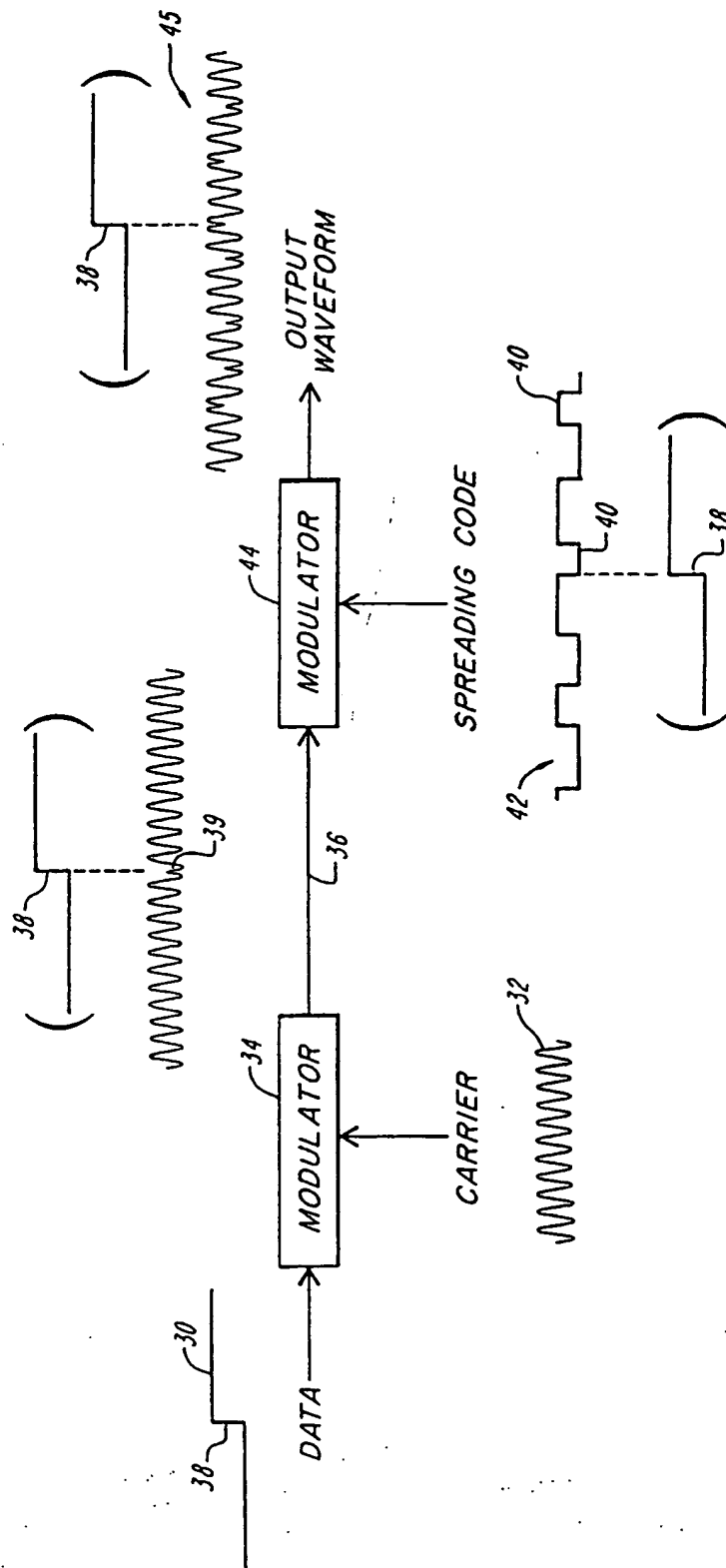
FIG. 3
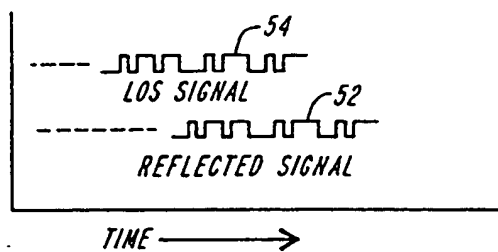
FIG. 5A
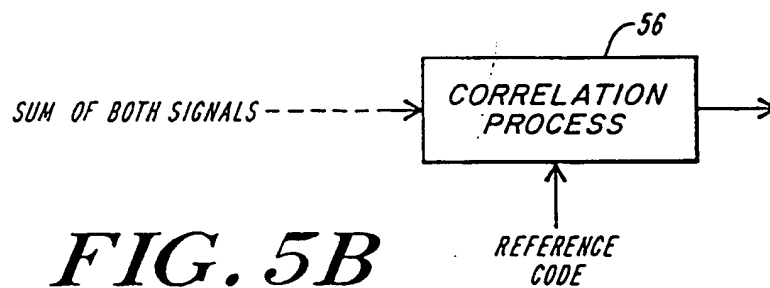
FIG. 5B
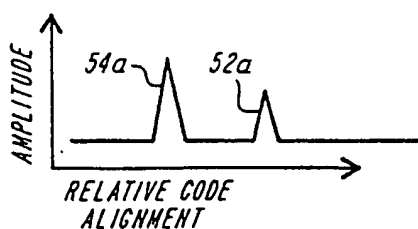
FIG. 5C
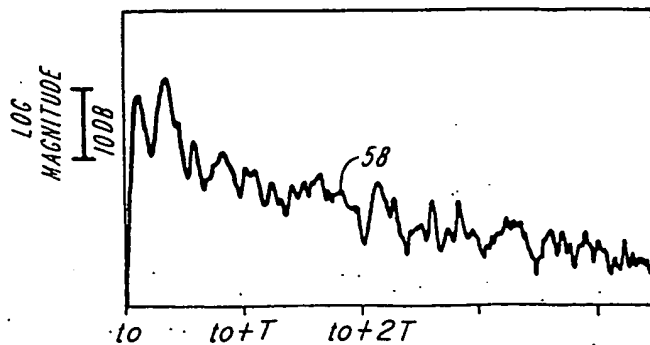
FIG. 6

REQUIRES FAST SYNCHRONIZER ?

	MESSAGE – SWITCHED	PACKET – SWITCHED	
		LONG	SHORT
TIME-SLOTTED	NO	NO	NO
RANDOM	NO	NO	YES

FIG. 7
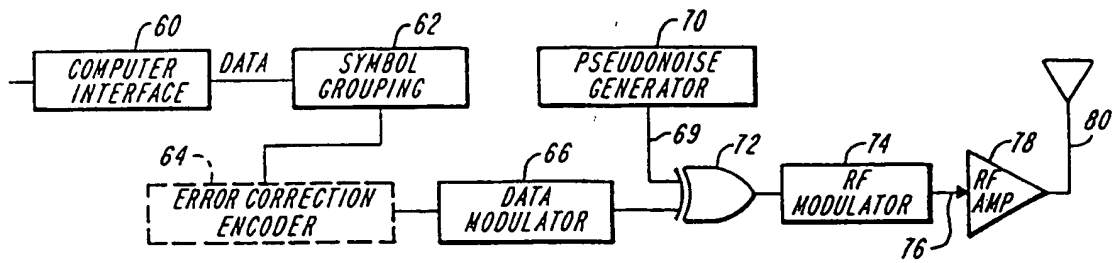
FIG. 8
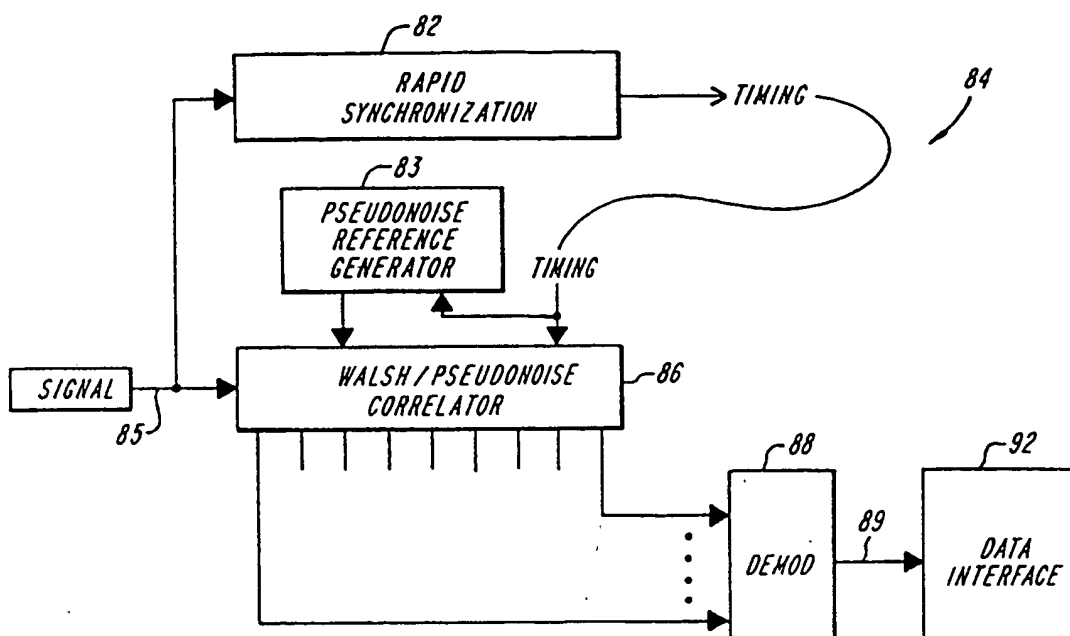
FIG. 9
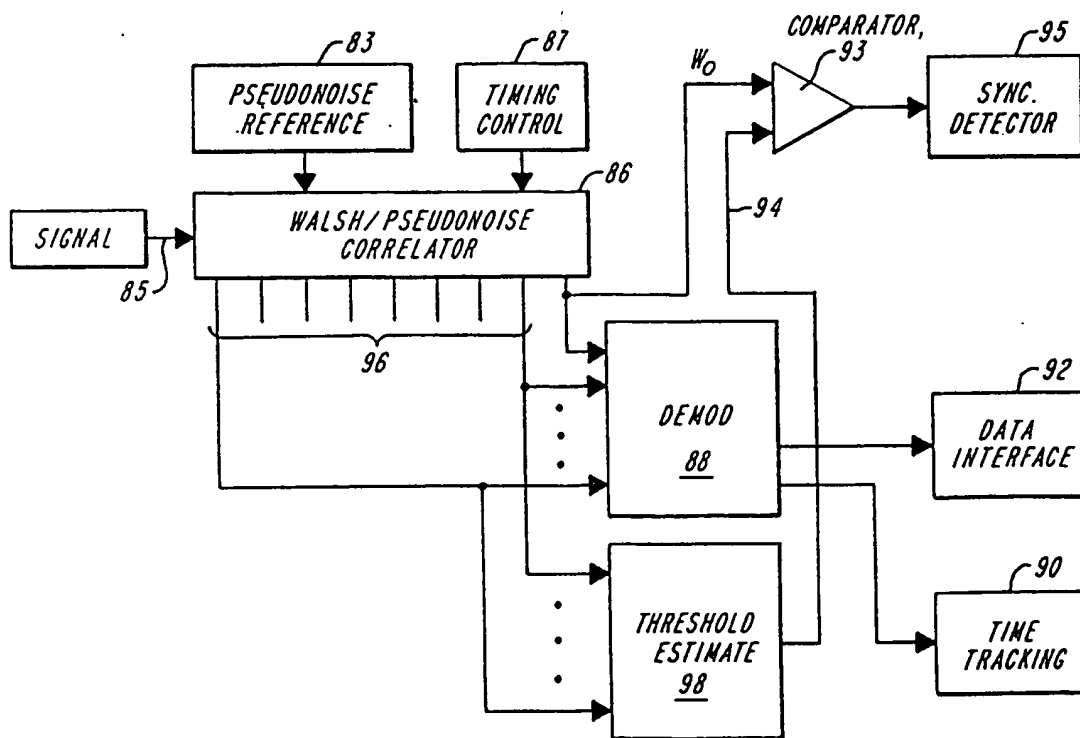
FIG. 10
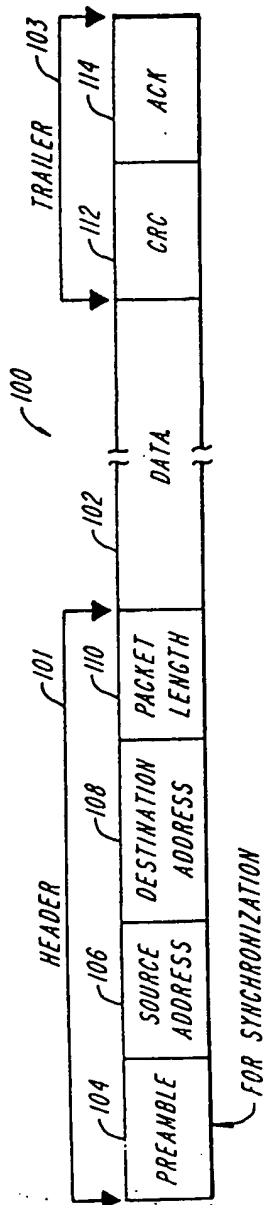
FIG. 11
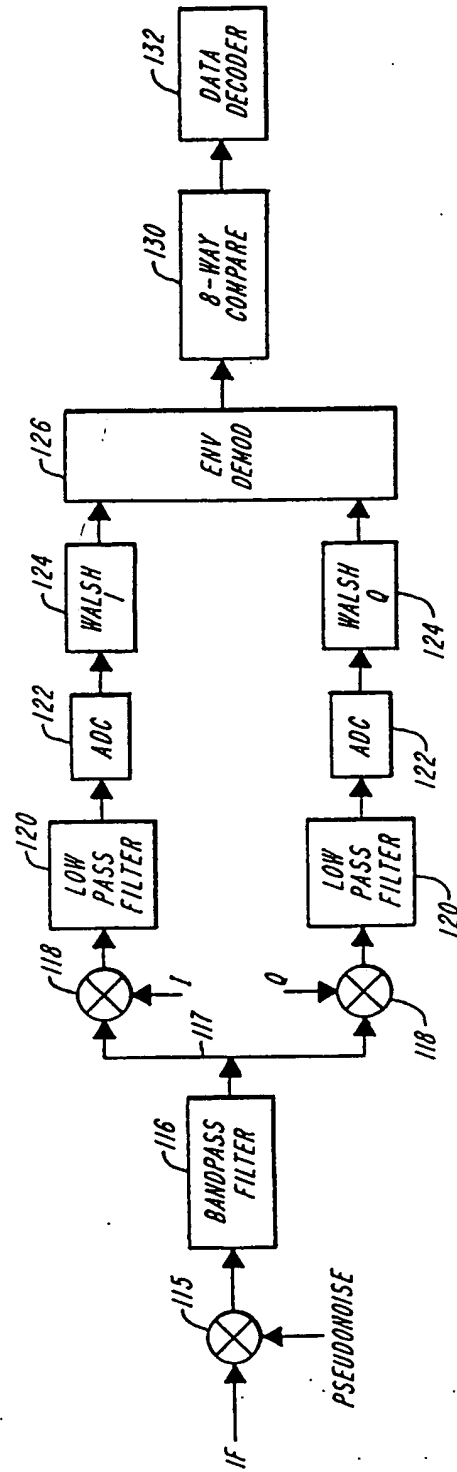
FIG. 12
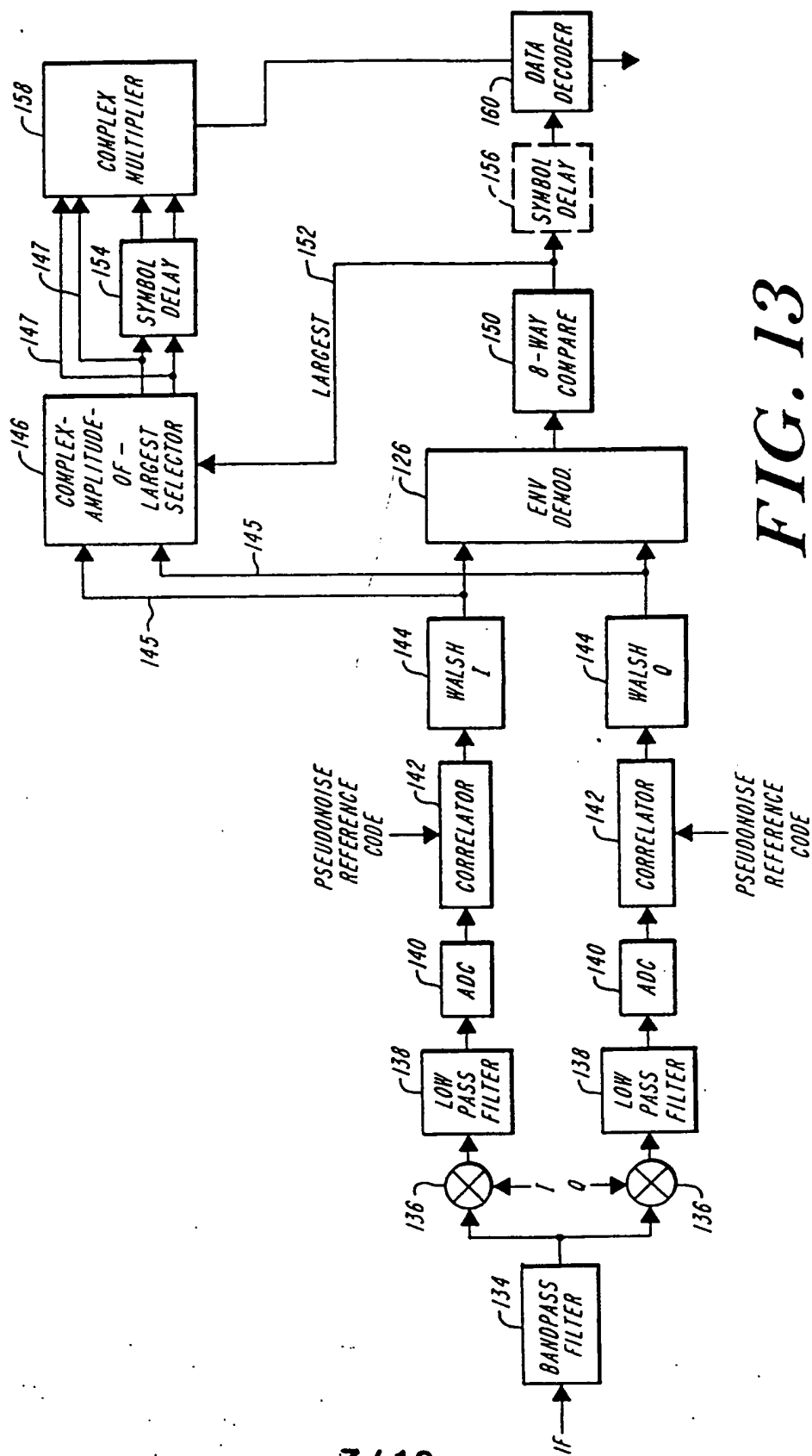
FIG. 13
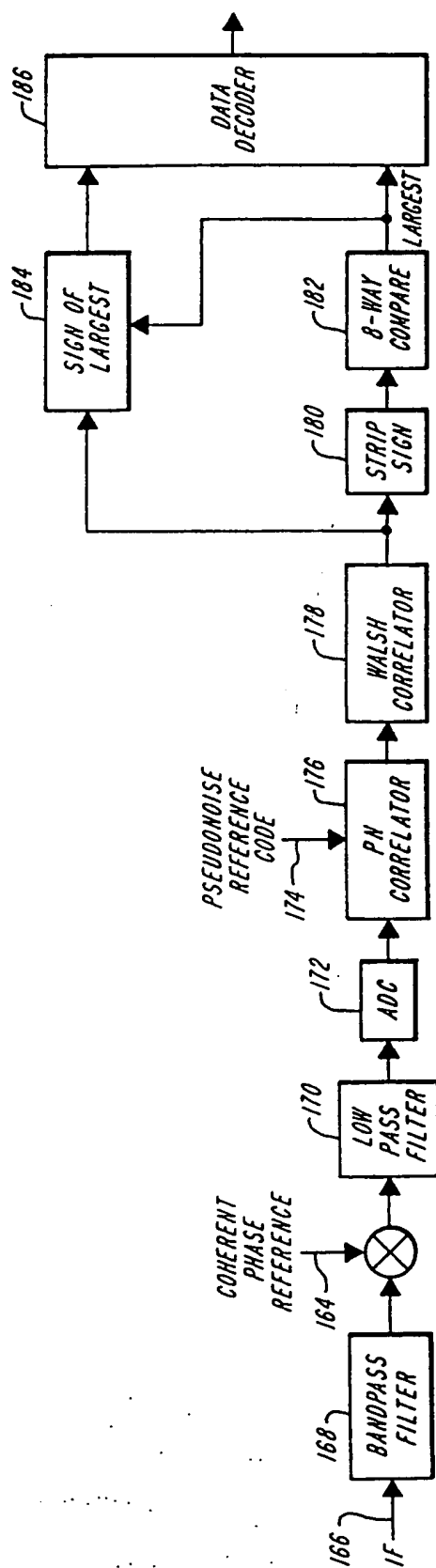
FIG. 14

WAL(0,t)

FIG. 15A

+1
0
−1
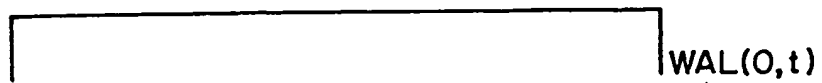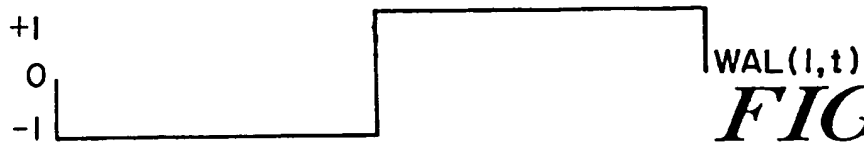
WAL(I,t)

FIG. 15B

WAL(2,t)

FIG. 15C

WAL(3,t)

FIG. 15D
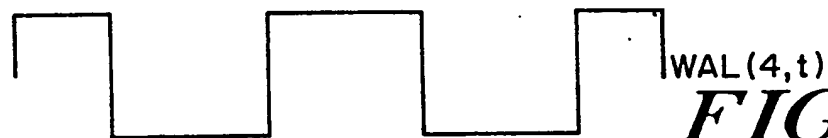
WAL(4,t)

FIG. 15E
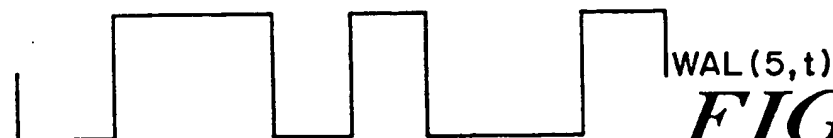
WAL(5,t)

FIG. 15F
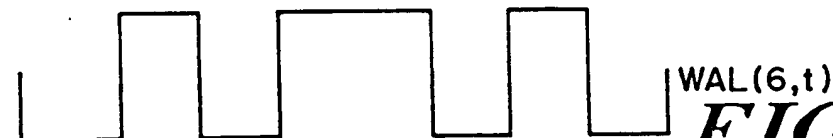
WAL(6,t)

FIG. 15G
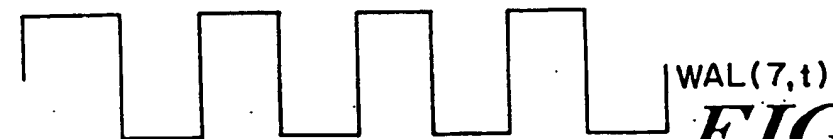
WAL(7,t)

FIG. 15H

FIG. 16

FIG. 17

SIGNAL SENSING ELECTRODES, 194

WALSH COMBINATION CIRCUITS, 198

DETECT/DATA DECODE, 202

SIGNAL SENSING ELECTRODES, 194

CLOCKING ELECTRODES

CHARGE STORAGE CELL, 193

201

MAGNITUDE AND M-WAY COMPARE, 200

190

195

194

SIGNAL CHARGE INJECTION

191

INPUT ELECTRODE 192
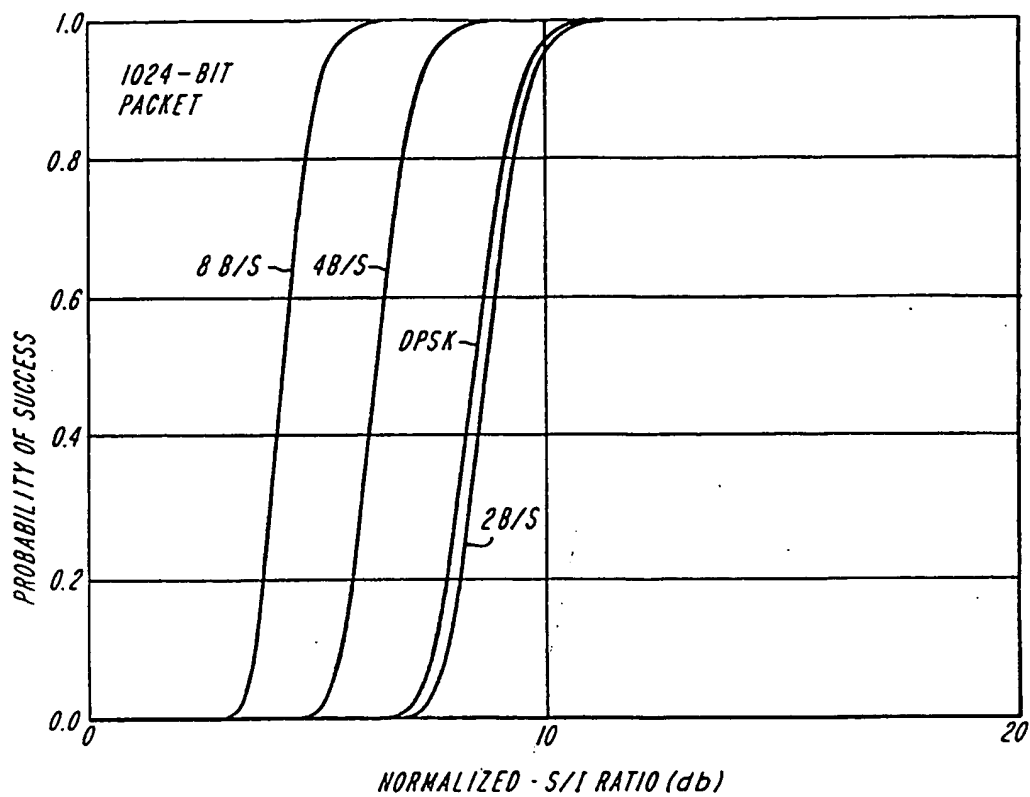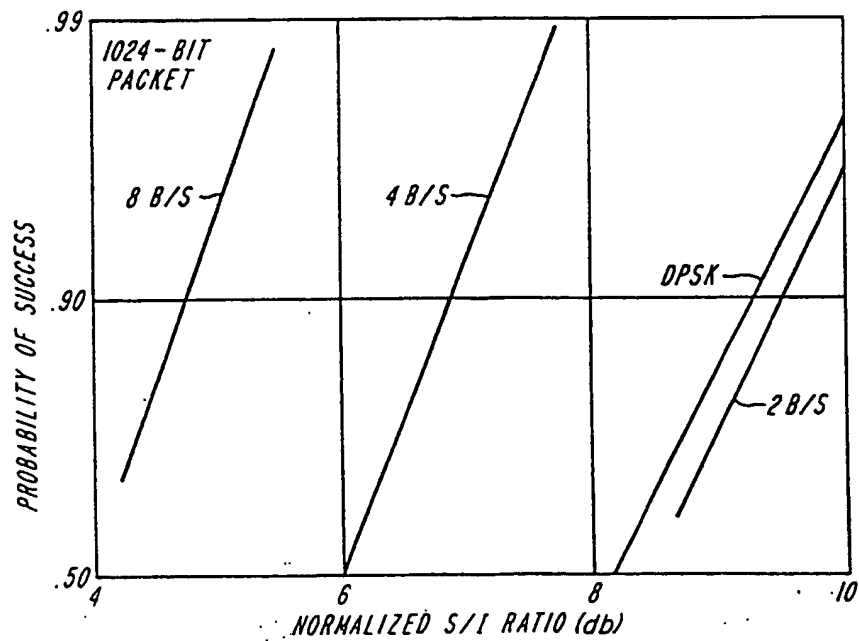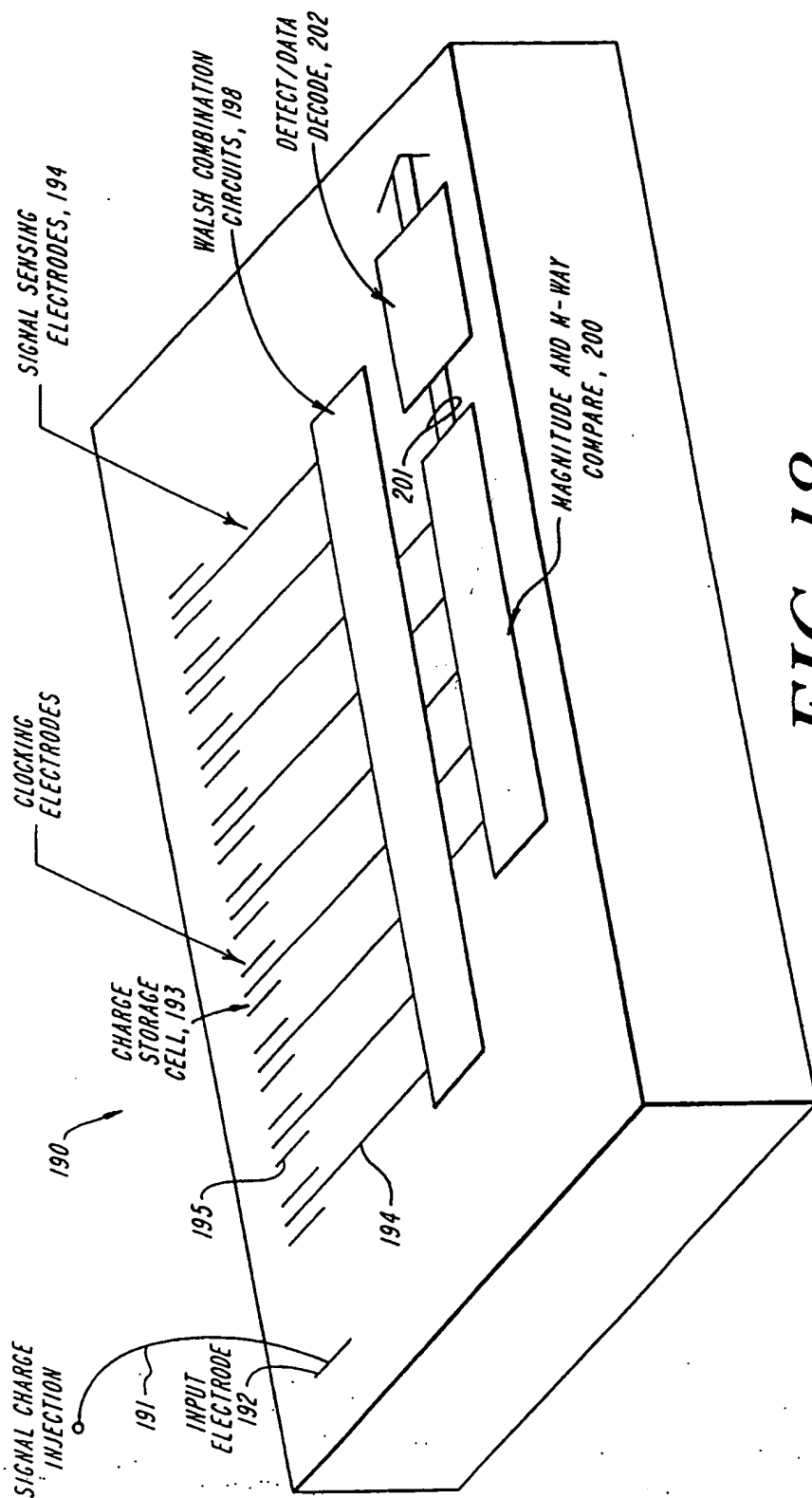
FIG. 18
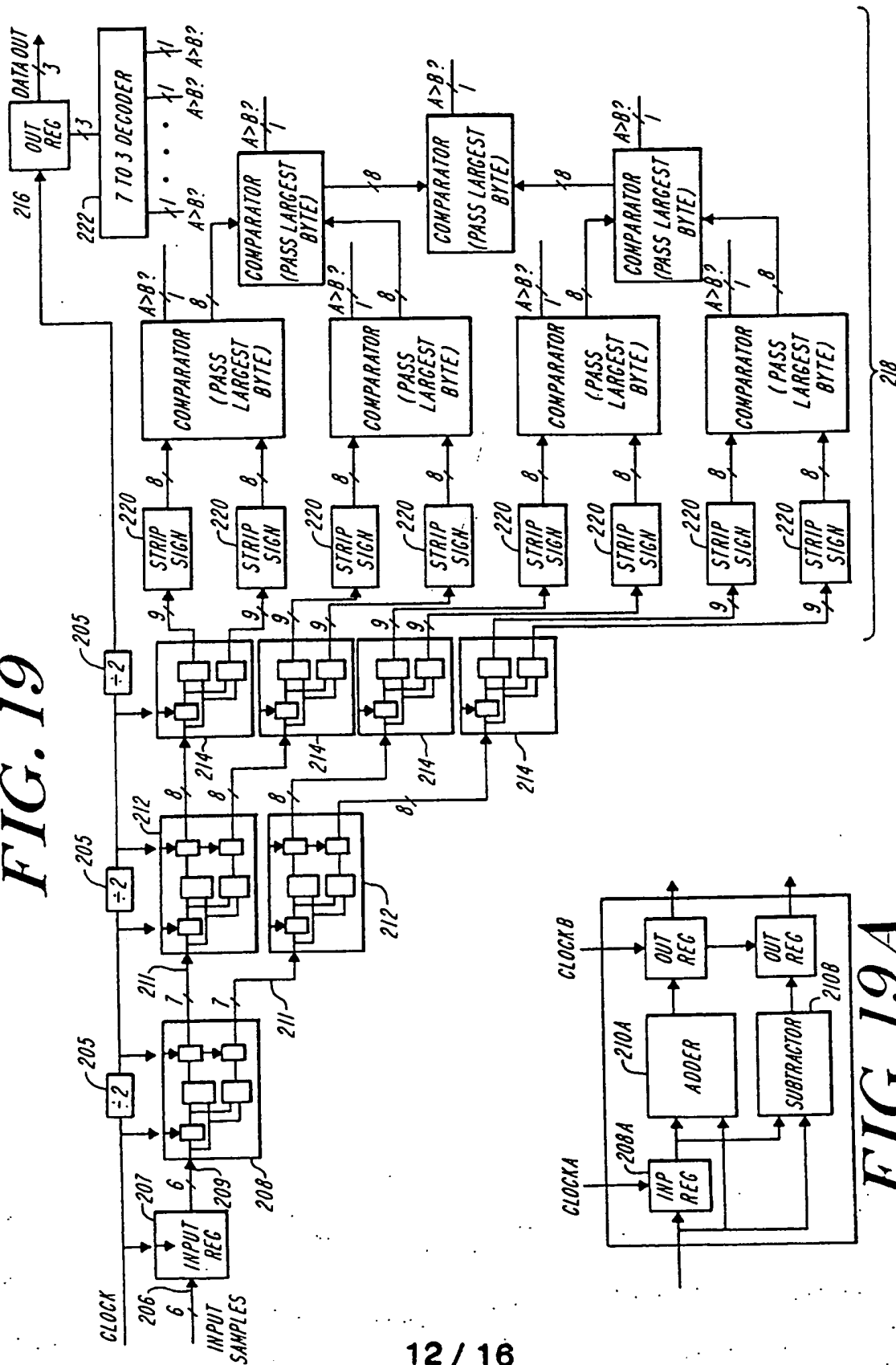
FIG. 19

FIG. 19A
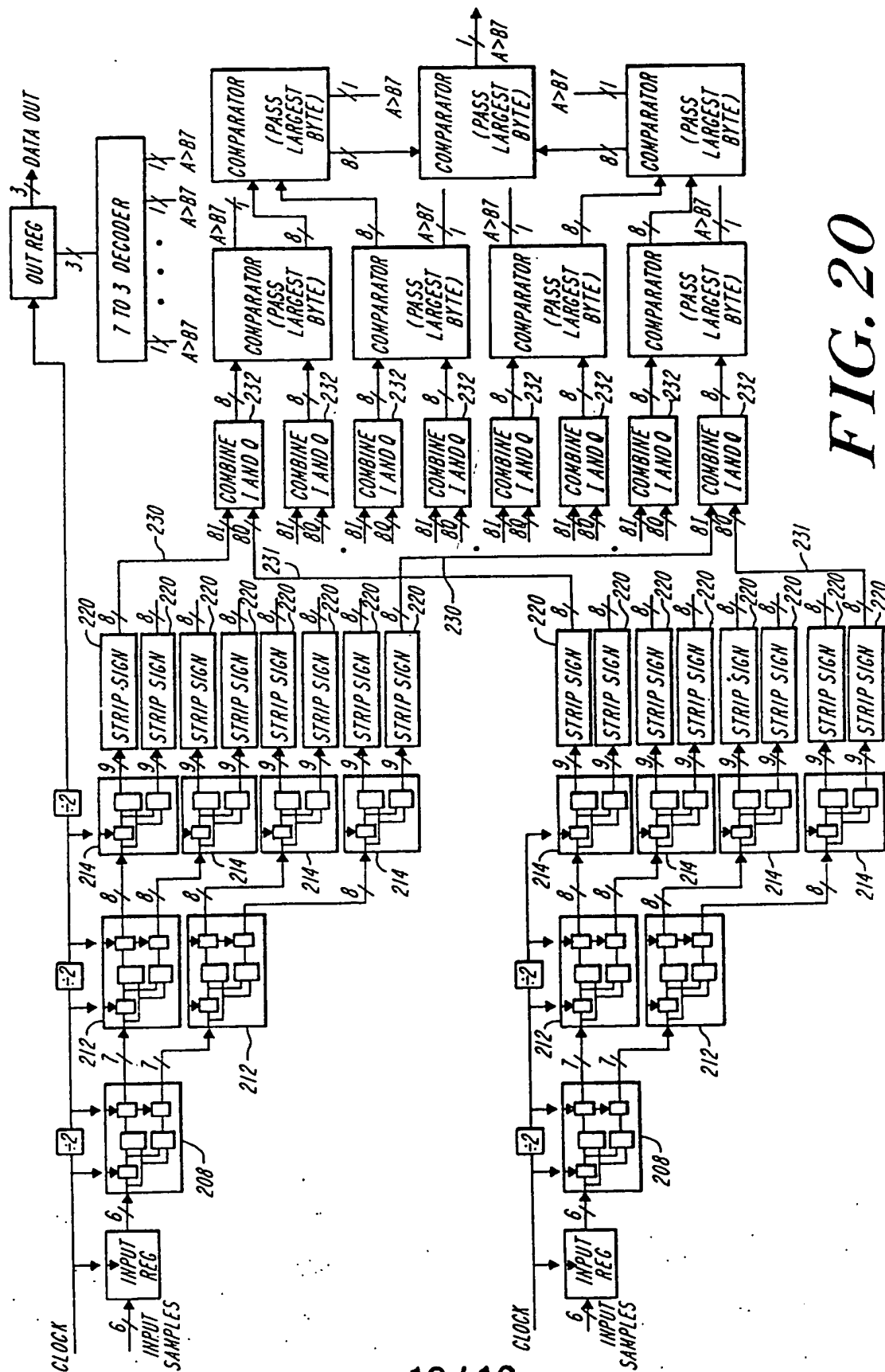
FIG. 20
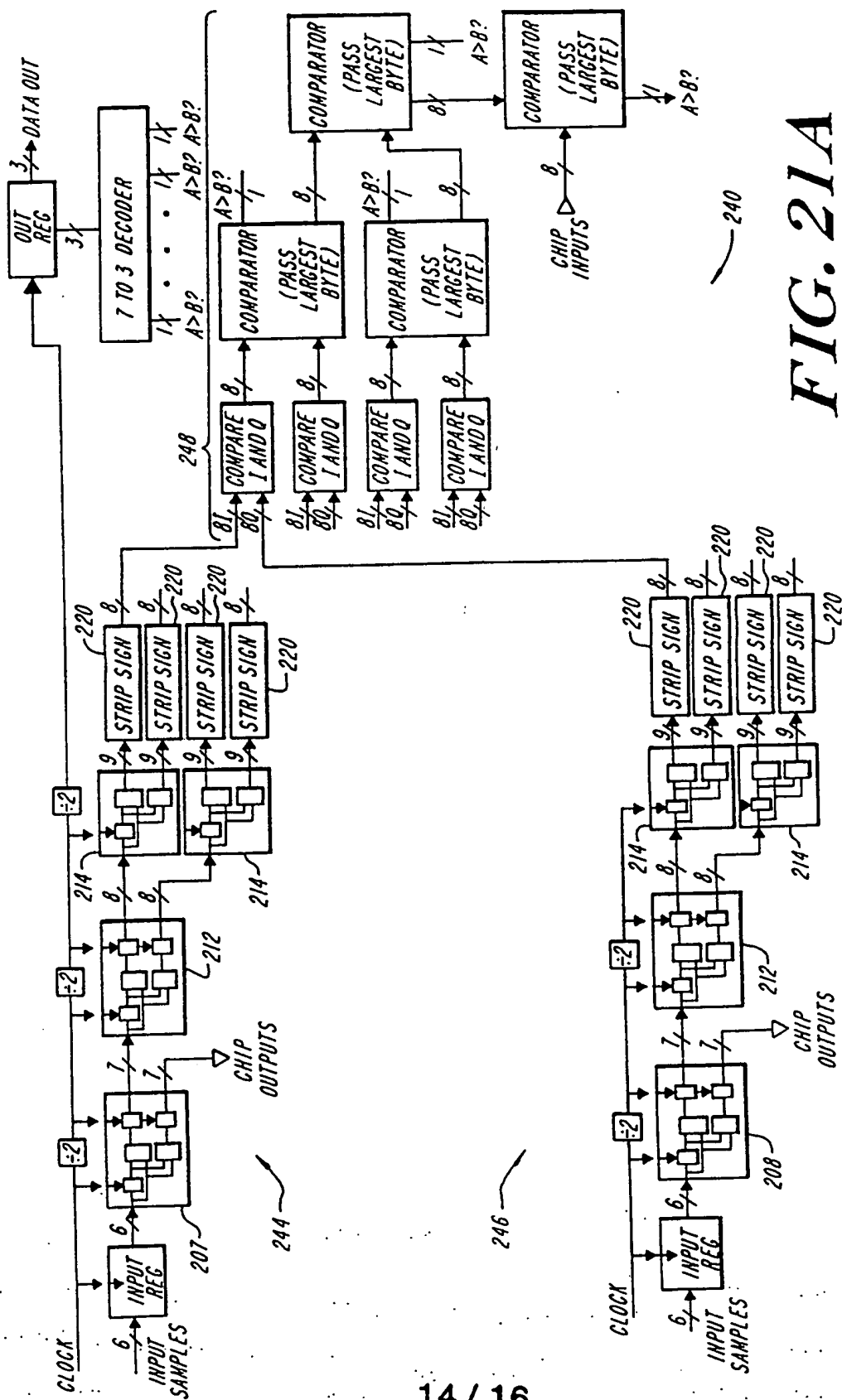
FIG. 21A
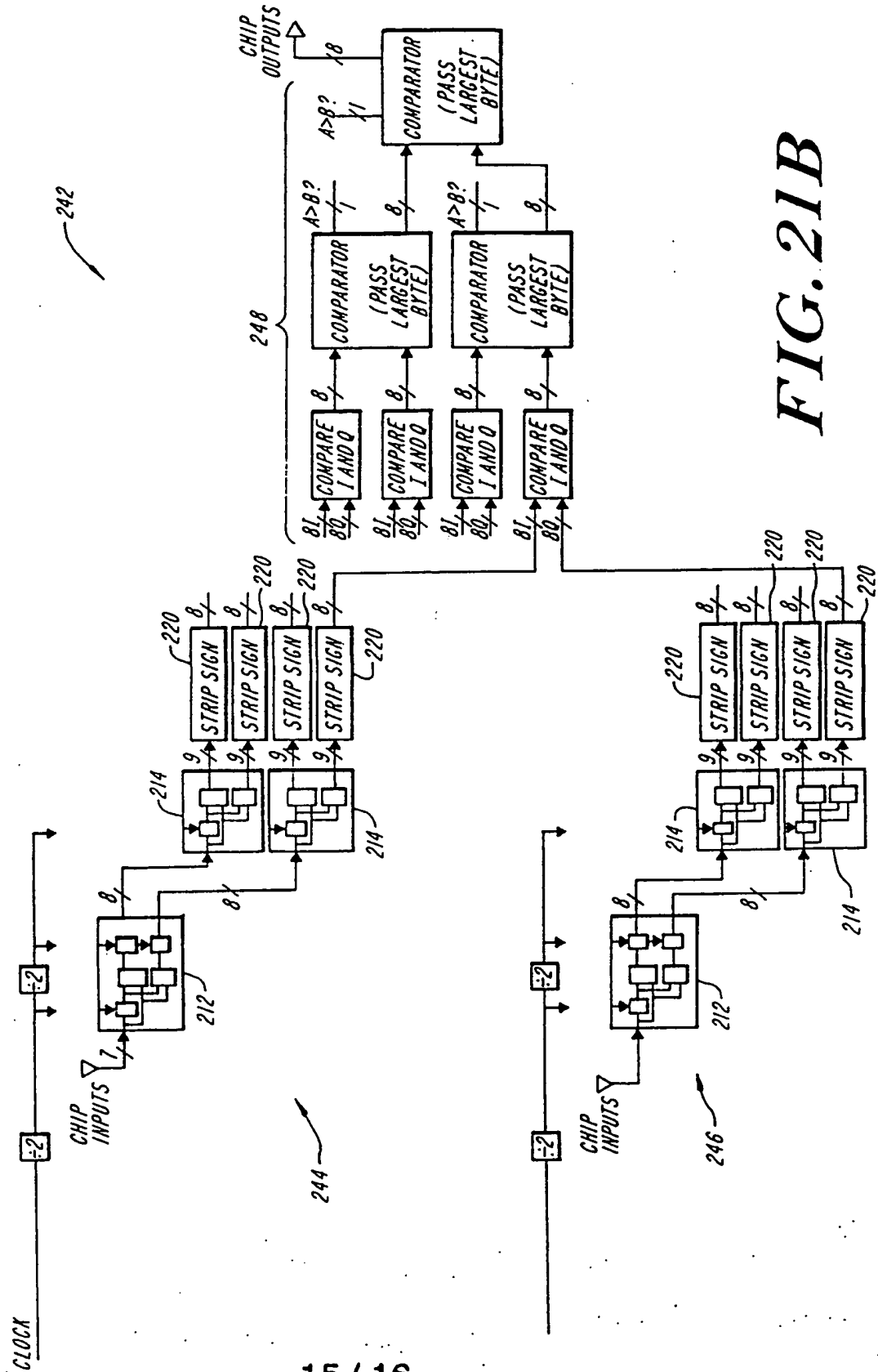
FIG. 21B
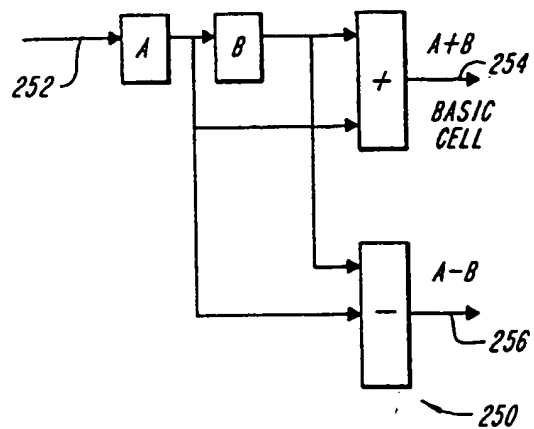
FIG. 22
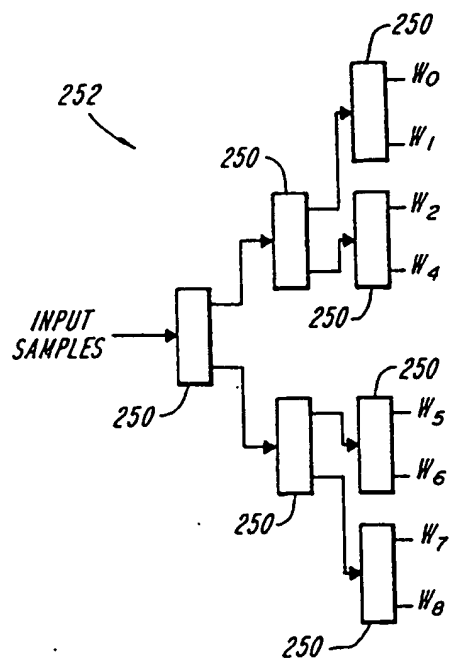
FIG. 23

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04B 1/707
US CL :375/1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,644,523 (HORWITZ) 17 FEBRUARY 1987; SEE FIG 1	1-83
A	US, A, 4,760,586 (TAKEDA) 26 JULY 1988	1-83
A	US, A, 4,894,842 (BROEKHOVEN ET AL.) 16 JANUARY 1990	

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 MARCH 1995	01 MAY 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer DAVID CAIN
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0511

Form PCT/ISA/210 (second sheet)(July 1992)*